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NONDISSIPATIVE SOLAR ARRAY OPTIMUM CHARGE REGULATOR

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1. SUMMARY OF EFFORT DURING THE ENTIRE PROGRAM

This report summarizes the progress during a one year program to study nondissipative solar array optimum charge regulators. These regulators are capable of efficiently coupling a spacecraft solar array to a spacecraft type battery. Efficient use of all power is necessary to minimize spacecraft size and weight. The method studied was that of maintaining solar panel operation at the maximum power point using nondissipative switching techniques.

During the first quarter, research in the area of optimum coupling and control techniques was performed in conjunction with the study of linear versus switching operation. Based on the study an extremal seeking controller was found to be the best means by which optimum power transfer could be realized. This type of control is utilized in the Surveyor spacecraft battery charge regulator. As a result of the study, a generalized design was presented, which was based on a switching regulator with an extremal seeking controller.

During the next three quarters of the program, this design was carried to completion with the construction of a 50-watt single phase regulator, and a 250-watt 2 phase regulator. Photographs of these units are shown in Figures 1-1 and 1-2. Complete testing of these two units were done during the last two quarters. These tests were run to verify the theoretical design and to insure proper operation over all possible environmental extremes. Testing was performed over a temperature range of $-40^{\circ}C$ to $+70^{\circ}C$.

In addition to the circuit study, research was performed to determine the types of battery systems that could be effectively utilized. Orbital conditions were derived and batteries were selected which would meet the given performance requirements. Battery charge devices to permit sensing of optimum charge were also investigated.

Three types of batteries were selected for evaluation. These were silver cadmium, silver zinc, and nickel cadmium. The charging efficiency of these batteries was tested as a function of a-c and d-c charging current in order to determine the effects on their performance.

In order to facilitate the testing of the regulator circuits, a solar panel simulator and a battery simulator were constructed. These units were designed to provide all of the conditions specified to test the regulators for proper operation.

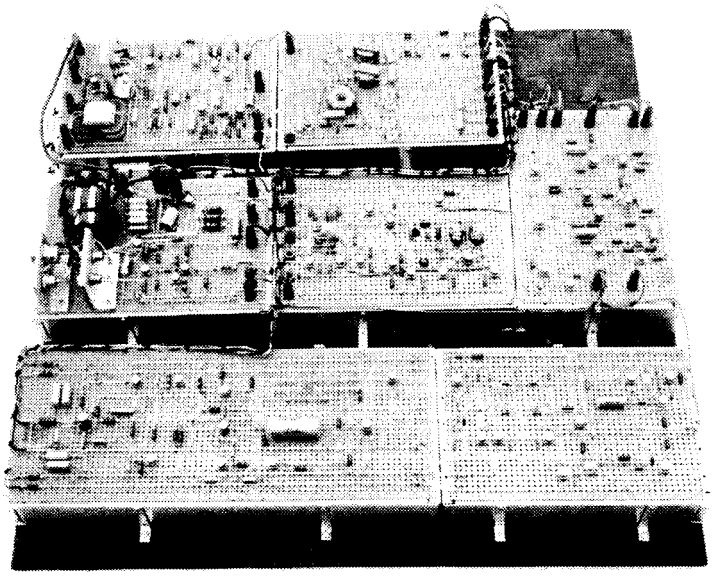


Figure 1-1. 50-watt OCR breadboard.

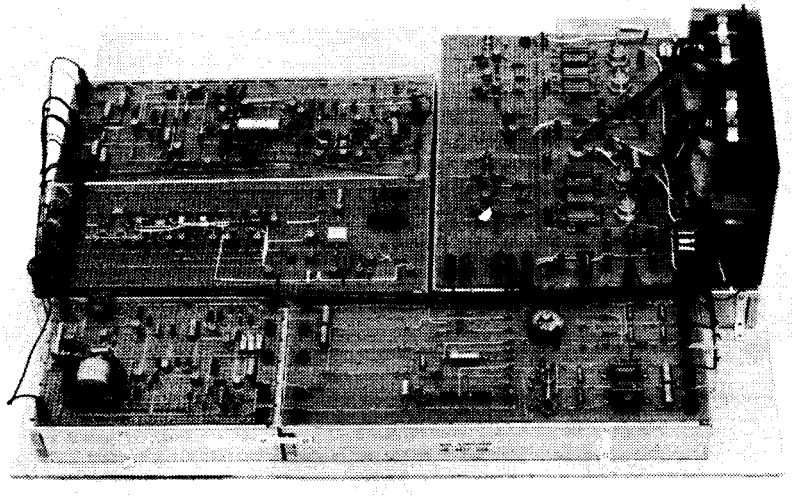


Figure 1-2. 250-watt OCR breadboard.

1.1 SUMMARY OF RESULTS

Complete testing of the 50-watt and 250-watt regulators indicated stability of operation over all of the extremes of input/output conditions and environment. In particular operation of 50-watt unit during the - 30 percent power transient was very satisfactory. Stable tracking of the maximum power point during this condition was observed. Noise immunity of both regulators was observed to be very high and switching loads on their outputs had no effect on operation.

Power transfer efficiency of the breadboard models was somewhat less than desired. For the 50-watt regulator, the 80-percent efficiency goal could be met by proceeding with the proposed improvements as described in Section 4.2. In the case of the 250-watt regulator, losses in the switching choke were found to be the prime contributor in causing the efficiency to fall below the goal of 90 percent. Further study of this problem will be made during the advanced program.

Comparison of actual circuit operation with the theoretical model indicated close correllation between the measured operating parameters and those calculated from the design equations.

The battery study indicated that a-c charging currents had very little or no effect upon battery efficiency. Charging currents of various frequencies were used on the three types of cells tested and there appeared to be no loss of charging efficiency due to these a-c variations.

AUTHOR

1.2 GENERAL DISCUSSION

Before proceeding to the design section, it is necessary to establish criteria for determining whether an optimum charge regulator would be of benefit to a given system. Basically this reduces to the problem of answering the question: Is the size and weight of a system without an OCR greater than that with an OCR? Power system size and weight can be related to efficiency since the solar panel size would have to increase as the coupling efficiency for a specified battery load decreased. Also, as the efficiency decreased, the system thermal design problems would be increased. A larger radiator would be required to solve this problem.

With unit emissivity and no solar loading, one square foot of radiator can transfer 57.3 watts to space. The associated weight factor is 244 lbs/kw. This assumes a radiator temperature of 50°C. A typical solar panel has a weight of 230 lbs/kw. For a 50 percent efficient system required to deliver 50 watts to a battery, the associated weight increase due to this inefficiency would be 23.2 pounds. For an equivalent battery load, if an 80-percent efficient OCR were employed, then a 6-pound increase in solar panel and radiator weight would be required. The weight of the OCR would be about 5 pounds. This would represent a weight savings of 12.2 pounds over the 50-percent efficient system.

On the other hand, if the solar panel maximum power point over its entire life did not vary considerably, it would be more efficient to tailor the solar panel and battery to each other and direct couple them. The tradeoffs are many and vary from system to system but it is evident that efficiency is a prime factor.

2. TECHNICAL DISCUSSION

This section is devoted to developing the design criteria associated with the concept of power transfer and control. It describes the method of transferring power from the solar panel to the battery, and also describes the technique for optimum control. The design equations for determining all critical circuit parameters are derived.

The basic power transfer and control is performed by a system which can be described by the block diagram of Figure 2-1. The solar panel is coupled to the battery by the power switching circuit. The power transferred by the switching circuit is a function of its switching duty cycle which is controlled by the optimum controller. It senses the battery current and modifies the duty cycle of the switching circuit in a manner which maximizes the battery current.

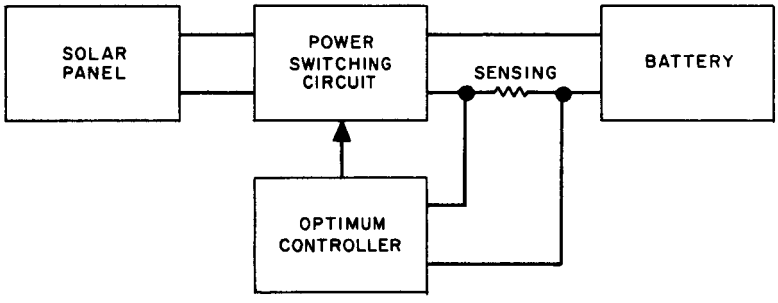


Figure 2-1. Generalized system block diagram.

2.1 POWER TRANSFER MECHANISM

The basic mechanism for efficient power transfer from the solar panel to the battery is that of energy storage in an inductor during the first portion of a switching cycle and then the release of this energy to the battery during the next portion of the cycle. The basic switching circuit is shown in Figure 2-2. Q1 is driven by a fixed frequency-variable duty cycle square wave. As the duty cycle is changed, the amount of energy stored in the choke each cycle is changed.

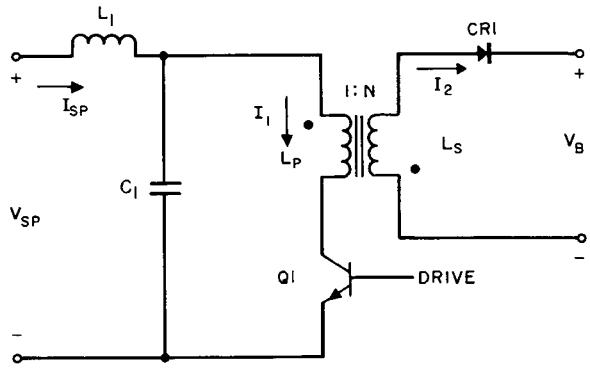


Figure 2-2. Basic switching circuit.

Figure 2-3 shows the current waveforms in both the primary and secondary of the switching choke. As shown by this figure, the current in L_p increases linearly as a function of time and it can be calculated from the relationship.

$$I_1 = \frac{V_{sp}}{L_p} t \qquad (2\text{-}1)$$

For a given duty cycle, D_1, the amount of energy stored in the choke during a single period of oscillation, T, is given by

$$E = 1/2\ L_p \left(\frac{V_{sp}}{L_p} D_1\ T\right)^2 = 1/2\ \frac{V_{sp}^2\ D_1^2\ T^2}{L_p} \qquad (2\text{-}2)$$

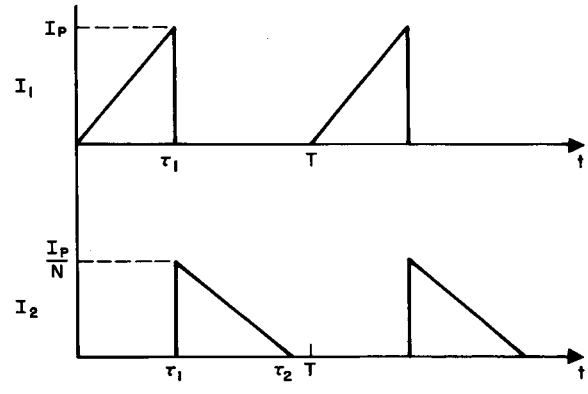


Figure 2-3. Switching circuit current waveforms.

If the energy stored during each cycle is given by the above relationship, then the power absorbed by the choke, and finally delivered to the battery is given by

$$P = E/T = 1/2 \frac{V_{sp}^2 D_1^2 T}{L_p} \tag{2-3}$$

Since,

$$T = \frac{1}{f_s} \tag{2-4}$$

where f_s = switching frequency,

then

$$P = 1/2 \frac{V_{sp}^2 D_1^2}{L_p f_s} \tag{2-5}$$

This relationship defines the amount of power drawn from the solar panel by a single phase regulator such as the 50-watt unit, which was the basis for one of the actual designs. From this equation the solar panel output current can be derived.

Since

$$P = V_{sp} I_{sp} \tag{2-6}$$

then

$$I_{sp} = 1/2 \frac{V_{sp} D_1^2}{L_p f_s} \tag{2-7}$$

As shown in Figure 2-3, the secondary current, I_2, is a linearly decreasing ramp beginning at the moment Q_1 turns off. The peak current of this ramp is determined by the peak current of I_1 and the turns ratio of the switching choke. The slope is a function of the battery voltage and the secondary inductance L_s.

$$I_2 = \frac{V_B}{L_s} (t - \tau_1) \tag{2-8}$$

If circuit losses are neglected, then the power delivered to the battery will be equal to the power drawn from the solar panel.

Therefore,

$$P = \frac{L_s I_2^2}{2T} \tag{2-9}$$

For a given duty cycle $D_2 = (\tau_2 - \tau_1)/T$. The amount of power delivered to the battery is given by

$$P = \frac{V_B^2 D_2^2}{2 L_s f_s} \tag{2-10}$$

From this relationship the average current flowing into the battery is found to be

$$I_2 (AVG) = \frac{V_B D_2^2}{2 L_s f_s} \tag{2-11}$$

The relationship derived in this section define the input and output functions for a single phase switching circuit. These relationships are summarized in Table 2-1. For a multiple phase circuit, the relationships of Table 2-1 can be utilized on a per phase basis. Table 2-2 summarizes the input/output relationships for a multiple phase regulator. The number of phases is given by the symbol ϕ. If $\phi = 1$, the equations of Table 2-1 can be seen to result.

Primary	Secondary
$P = \frac{V_{sp}^2 D_1^2}{2 L_p f_s}$	$P = \frac{V_B^2 D_2^2}{2 L_s f_s}$
$I_{sp} = \frac{V_{sp} D_1^2}{2 L_p f_s}$	$I_2(AVG) = \frac{V_B D_2^2}{2 L_s f_s}$
$I_1(peak) = \frac{V_{sp} D_1}{L_p f_s}$	$I_2(peak) = \frac{I_1(peak)}{N}$

Table 2-1. Single phase switching circuit input/output relationships.

Primary	Secondary
$P = \frac{V_{sp}^2 D_1^2}{2 L_p f_s} \phi$	$P = \frac{V_{sp}^2 D_1^2}{2 L_s f_s} \phi$
$I_{sp} = \frac{V_{sp} D_1^2}{2 L_p f_s} \phi$	$I_2(AVG) = \frac{V_B D_2^2}{2 L_s f_s} \phi$
$I_1(peak) = \frac{V_{sp} D_1}{L_p f_s}$	$I_2(peak) = \frac{I_1(peak)}{N}$

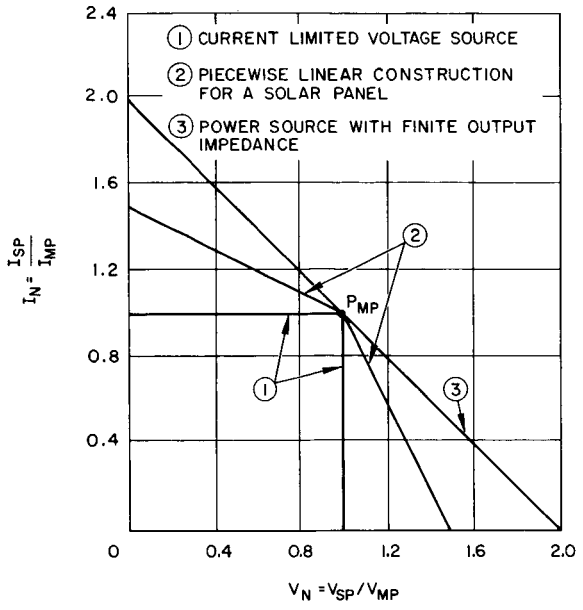
Table 2-2. Multiple phase switching circuit input/output relationships.

The filter L1-C1 is provided to average the switched current I_1. This allows the solar panel to operate at a relatively fixed voltage and current.

2.2 OPTIMUM POWER CONTROL

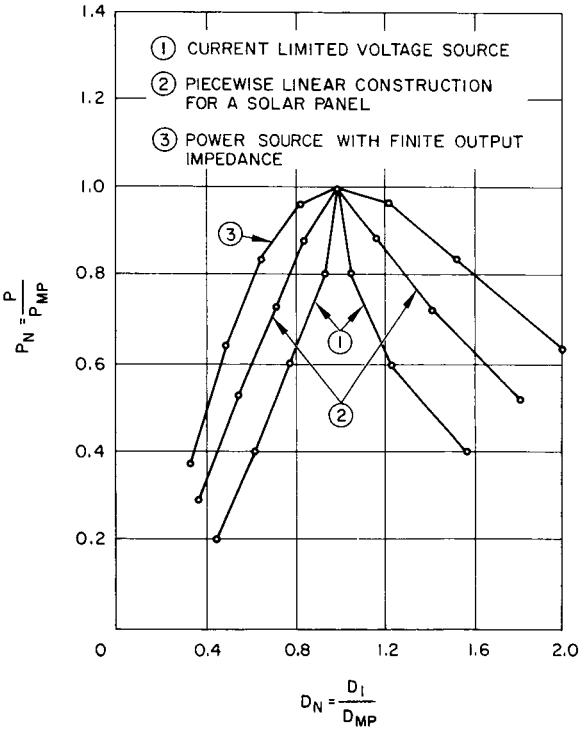
Based on the relationships derived in the last section and summarized in Tables 2-1 and 2-2, it can be seen that the power transferred from the solar panel to the battery will be a function of the duty cycle of Q1. Also of importance is the V-I characteristic of the power source as this will determine the manner by which the power varies as a function of duty cycle.

Figure 2-4 is a plot of the idealized V-I characteristics of various types of power sources. The curves are normalized with respect to the maximum power point. Curve 1 is a representation of a current limited voltage source and curve 3 is that of a voltage source with a finite series impedance. Curve 2 is representative of a multitude of characteristics which could be drawn between the extremes of 1 and 3. Of particular interest is the fact that practical solar panel output characteristics are somewhat between the limits of 1 and 3.



NOTE: V_{MP} AND I_{MP} ARE VOLTAGE AND CURRENT AT THE MAXIMUM POWER POINT

Figure 2-4. Normalized V-I characteristic for various types of power sources.



NOTE: P_{MP} AND D_{MP} ARE VALUES AT THE MAXIMUM POWER POINT

Figure 2-5. Normalized plot of power versus duty factor for the power sources of Figure 2-3.

If all of the parameters are normalized with respect to their values at the maximum point, P_{mp}, as shown in Figure 2-4, then

$$P_n = \frac{P}{P_{mp}} = V_n^2 D_n^2 \tag{2-12}$$

where

$$V_n = V_{sp}/V_{mp}$$

$$D_n = D_1/D_{mp}$$

A normalized plot of power versus duty factor is shown in Figure 2-5 for curves 1, 2, and 3. Curve 1 exhibits the most radical change of power for a duty factor variation, while curve 3 shows the most gradual. These curves indicate that in order to maintain very low hunting losses it will be necessary to keep the duty factor variations during the hunting cycle below about 5 percent of D_{mp}. Hunting is the term used for describing the oscillation of the regulator about the maximum power point.

As shown by Figure 2-5, as the duty factor is increased from zero the maximum power point is eventually reached. After this point the power will begin to decrease again. In terms of the power delivered to the battery,

$$P = V_B I_B \tag{2-13}$$

where V_B is the battery voltage and I_B is the average output current of the regulator. Since it is assumed that V_B is a constant for periods of time much greater than the hunting period, the power output is directly proportional to the output current, I_B. Therefore, as the duty factor is changed, the average output current will remain directly proportional to the input power and it will vary in the manner described in the diagram of Figure 2-5. In other words the normalized power may be written as:

$$P_n = KI_B/I_{mp} = KI_n \tag{2-14}$$

where K is a constant of proportionality.

Because of this relationship, the output current may be sensed to determine when the regulator is operating at the maximum power point.

2.3 BASIC REGULATOR OPERATION

Based on the results of the preceding section, it can be seen that if the duty factor of the switching circuit is properly adjusted, then the regulator can deliver the maximum available power from the solar panel at all times. It was also shown that the controlling parameter is the average battery current since it is proportional to power. Therefore, a controller which senses the output current and uses this information to control the duty cycle of the switching circuit is the basis for the design.

As shown by the block diagram of Figure 2-6, the control loop which adjusts the duty factor of the switching circuit to the proper value consists of five functional blocks. The output waveforms for each of these blocks are shown in Figure 2-7 and they will be referred to in the following discussion.

If at time t = 0, the regulator is operating at point P_1 of the solar panel characteristic shown in Figure 2-8, and the duty factor is decreasing, the following events will occur. The average value of current flowing into the battery is shown in Figure 2-7a at P_1, and it is increasing towards I_{mp}. At the time that the operating point passes P_{mp} on the solar panel characteristic, the average battery current will reach a maximum and then begin decreasing. The battery current is sensed by a small resistor and then this voltage is amplified by the current sensing amplifier (CSA). The CSA has a low pass characteristic so that it amplifies the average battery current and rejects the switching (carrier) frequency component. The output of the CSA is then fed to the peak holding comparator (PHC) which compares the peak value of the CSA's output to its instantaneous value. When the CSA output has dropped a predetermined ΔV below its peak, a pulse, V_{phc}, is generated as the output of this circuit. This corresponds to the point P_2 in Figure 2-8. The pulse generated by the PHC causes the

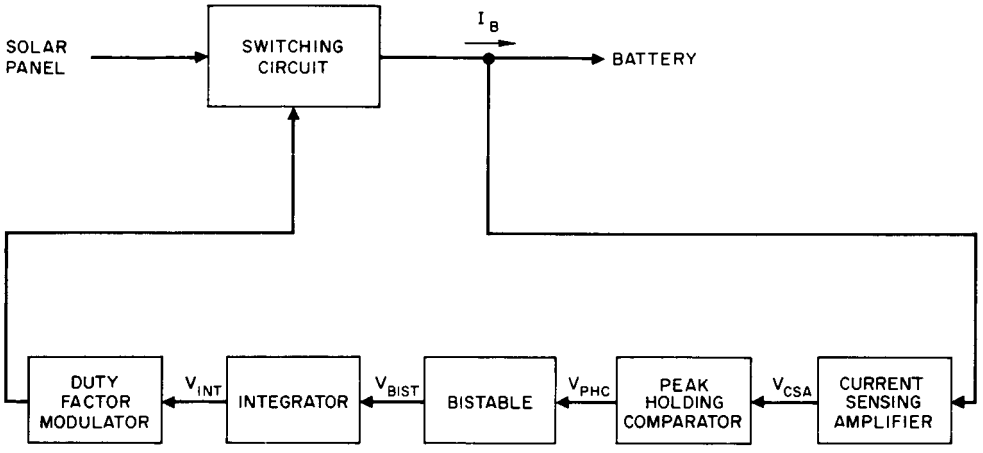


Figure 2-6. Optimum charge regulator block diagram.

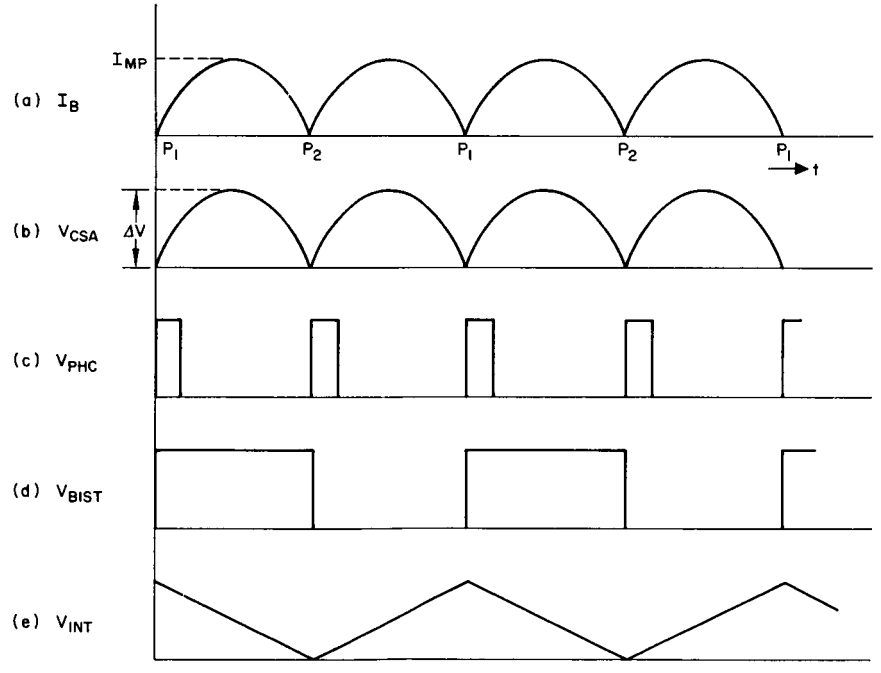


Figure 2-7. Optimum charge regulator control waveforms.

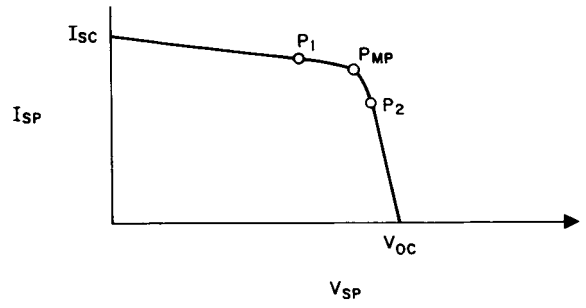


Figure 2-8. Solar panel V-I characteristic.

bistable to reverse states and this causes the integrator to begin increasing the duty cycle. The entire cycle is repeated as the regulator moves its operating point from P2 back to P1. A complete hunting cycle is from P1 through P2 and back to P1.

2.4 HUNTING FREQUENCY

The time required for the regulator to complete one cycle (P1 $\longrightarrow$ P2 $\longrightarrow$ P1) is termed the hunting period or inversely the hunting frequency.

If at time t = 0, the regulator is operating at the maximum power point then the power transferred by a multiple phase regulator can be written as

$$P = \frac{\phi V_{sp}^{2} D_1^{2}}{2 L_p f_s} = \frac{V_B I_B}{\eta} \qquad (2\text{-}15)$$

where

η = regulator efficiency

ϕ = number of phases.

If the duty factor now decreases a small amount then the change in battery current as a function of the change in duty factor and solar panel voltage can be approximated as

$$I_B = \frac{\phi V_{sp} D_1 \eta}{L_p f_s V_B} \left[D_1 \Delta V_{sp} + V_{sp} \Delta D_1 \right] \qquad (2\text{-}16)$$

ΔV_{sp} is a function of the solar panel characteristic and ΔD_1 is a function of the integrator and duty factor modulator circuits. Since the input to the integrator is a step function, its output will have the form

$$\Delta D_1 = kt \tag{2-17}$$

The units of ΔD_1 are volts/second/volt. This is true since the change in duty factor as a function of time is related to the integrator output as a percentage of the peak-to-peak change per switching cycle of the duty factor modulator comparator voltage.

Combining equations 2-16 and 2-17 and solving for the time required for the operating point to shift from P_{mp} to P_2 yields the result

$$t_{p2} = \frac{\Delta I_B L_p f_s V_B - D_1^2 \eta V_{sp} \Delta V_{sp}}{\eta V_{sp}^2 D_1 K\phi} \tag{2-18}$$

It must be noted that since both the duty factor and the average battery current are decreasing, there are negative signs associated with K and ΔI_B.

Assuming complete symmetry for each half cycle ($P_{mp} \longrightarrow P_2 \longrightarrow P_{mp}$ and $P_{mp} \longrightarrow P1 \longrightarrow P_{mp}$) the hunting frequency is found to be

$$f_h = \frac{\eta V_{sp}^2 D_1 K\phi}{4\left[\Delta I_B L_p f_s V_B - D_1^2 \eta V_{sp} \Delta V_{sp}\right]} \tag{2-19}$$

2.5 SWITCHING FREQUENCY SELECTION

There are several criteria for switching frequency selection. Selection of the proper frequency of switching is important because if it is too high efficiency will suffer, while if it is too low, size and weight will be the penalty.

Upon examination of the equations in Tables 2-1 and 2-2, it can be seen that the product of f_s and L_p occurs in all of them. With a given solar panel and a fixed maximum power point, if f_s is decreased, then

L_p must be increased or D_1 must be decreased in order to satisfy the equation. An increase in L_p means an increase in size and weight of this component. If D_1 is decreased, the peak current, I_1, increases which results in increased losses.

On the other end of the scale, if f_s is increased, L_p can be decreased thereby reducing its size and weight. However, there are two penalties which result in lowered efficiency. The first is due to increased core losses in the switching choke due to the increased frequency. The second is due to transistor switching losses. Since the main power transistor, Q_1, has an inductive load line when it turns "off", the waveforms of Figure 2-9 can be used to calculate the switching loss. From these it is found that

$$P_{sw} = I_1(\text{peak}) \left[V_{sp} + \frac{V_B}{N} \right] t_{sw} f_s \qquad (2\text{-}20)$$

where t_{sw} is the voltage rise time and the current fall time for Q_1.

Since t_{sw} is a constant for any given device, P_{sw} will increase as f_s increases. Therefore, proper selection of the switching frequency is necessary to optimize efficiency, size, and weight.

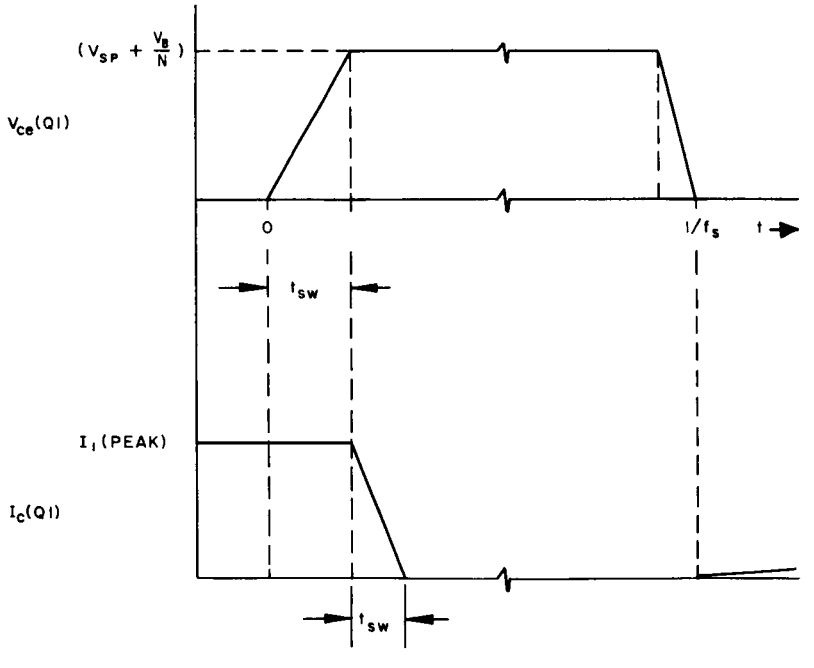


Figure 2-9.

Switching transistor waveforms for the switching loss calculation.

3. CIRCUIT DESIGN

Two separate cases were considered in the circuit design phase of this program. The first was a single phase regulator designed to operate from a 50-watt solar panel. The second was a two phase regulator designed to operate from a 250-watt panel.

The basic concept for both designs was similar except for the fact that the two phase scheme was used in the higher power regulator. This was done to improve the efficiency of this unit and also to improve the ripple filtering characteristics.

The following discussion will be concerned with the specific consideration for the design of the circuits for both cases. Table 3-1 summarizes the specifications for the design of both regulators.

3.1 CASE I: 50-WATT REGULATOR DESIGN

A functional block diagram of this regulator is shown in Figure 3-1. These blocks represent individual circuit functions and the following design discussion will concern itself with each block on an individual basis. In some cases each functional block will be broken down even further.

The method of determining the parameters for certain critical components, as well as a general circuit operation will be discussed.

3.1.1 Switching Circuit

In terms of overall system efficiency this circuit plays the most important part. Its function is to transfer the power from the solar panel to the battery. A schematic diagram of the entire switching circuit is shown in Figure 3-2.

The operation of this circuit proceeds as follows. If at $t = 0$, the duty factor modulator (DFM) input goes from -5 volts to +5 volts as shown in Figure 3-3a, then this signal will be amplified by the succeeding stages, thereby allowing Q1 to turn "on". As shown by the waveform of Figure 3-3b, the collector-emitter voltage of Q1 will go from V_{sp} to V_{ce} (sat) and the current in L_p will begin increasing

	Case I: 50 Watts	Case II: 250 Watts
Solar Panel Voltage	20 - 30 volts	40 - 50 volts
Solar Panel Current	2.5 - 1.67 amps	6.25 - 5.0 amps
Battery Voltage	12 - 20 volts	25 - 40 volts
Battery Current	3.33 - 2.0 amps	9.0 - 5.63 amps
Efficiency Goal	80 percent	90 percent
Switching Frequency (f_s)	10 khz	2 khz
Hunting Frequency (f_H)	150 - 300 hz	20 - 60 hz
Hunting Loss Goal	2 percent	2 percent
Power Transient	-30 percent	None
Transient Frequency	10 hz	None
Rise and Fall Time	10 - 20 msec	None
Duty Cycle	50 percent	None

Table 3.1. Summary of Specifications for both cases of the design.

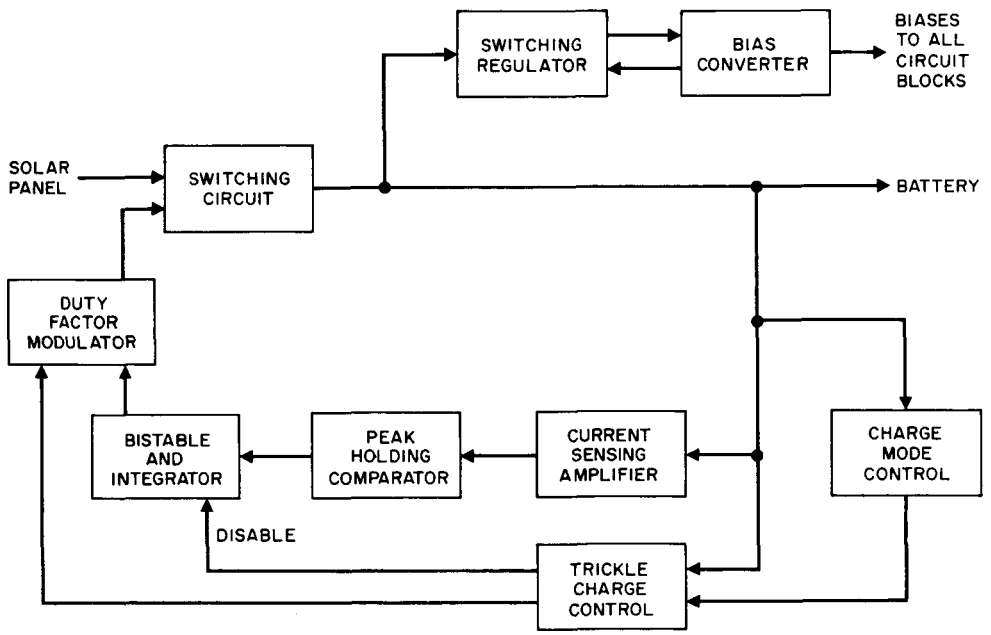


Figure 3-1. 50-watt OCR functional block diagram.

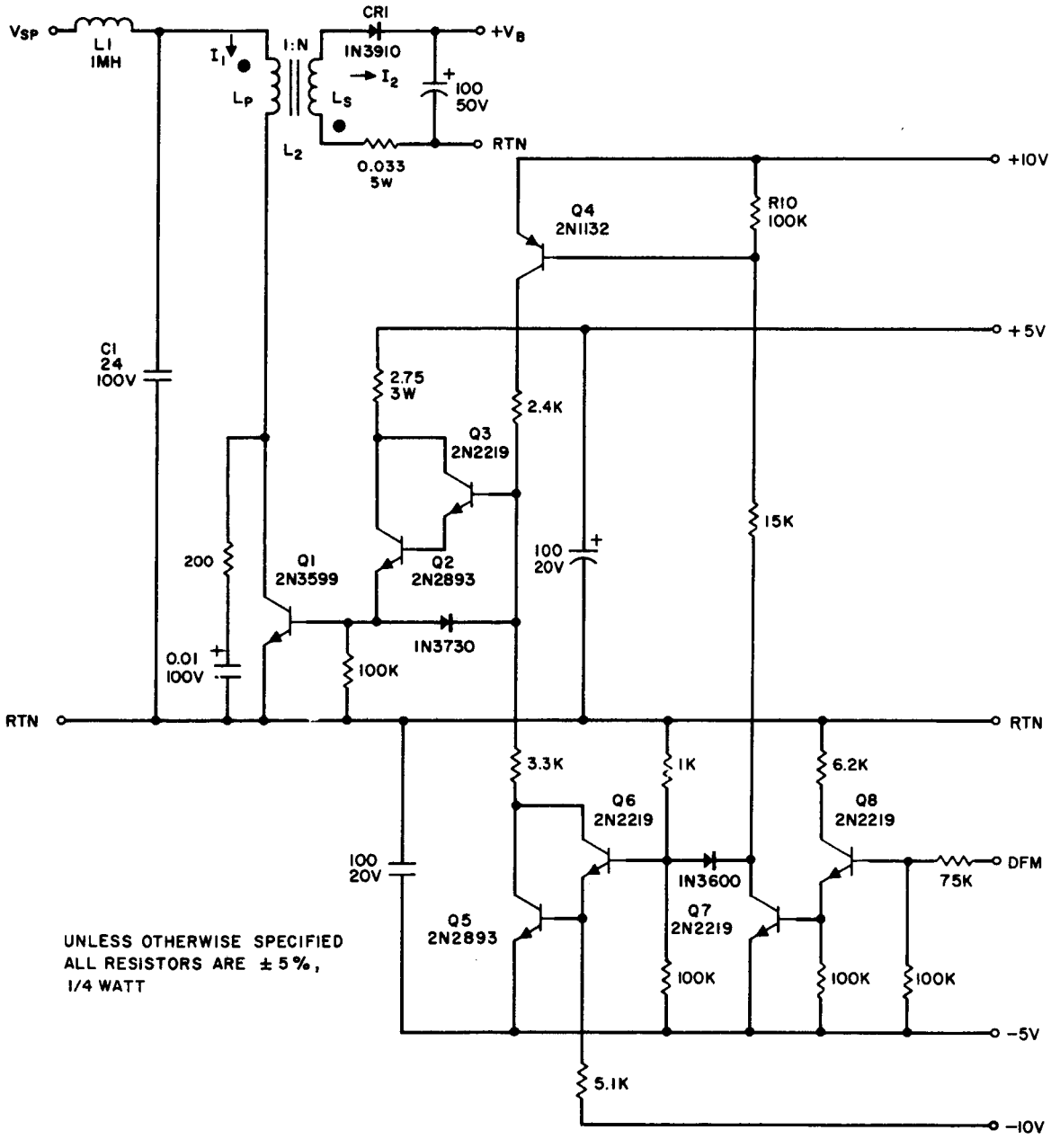


Figure 3-2. 50-watt switching circuit.

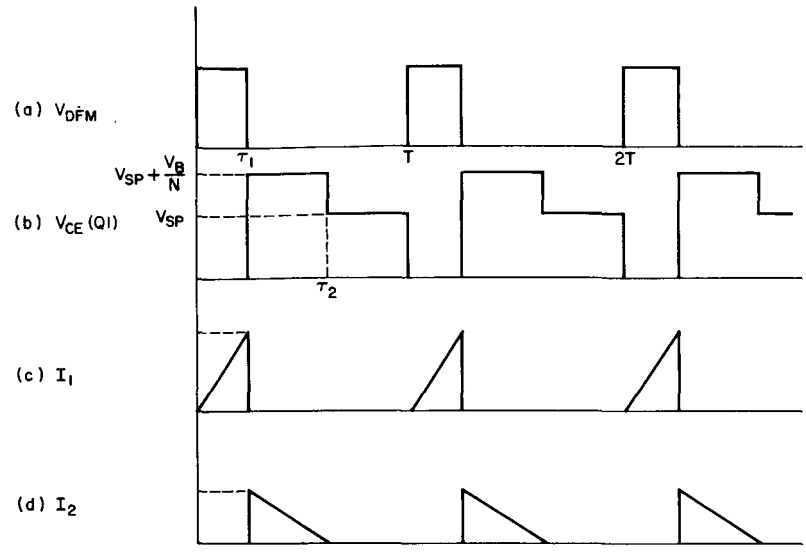


Figure 3-3. Single phase switching circuit waveforms.

linearly as shown in Figure 3-3c. At time τ_1, the duty factor modulator input returns to -5 volts. This allows Q5 to turn "on", thereby reverse biasing Q1 and turning it "off". During the "on" time of Q1, CR1 is reverse biased. When Q1 turns "off", the voltage across the secondary of L2 increases until it forward biases CR1 and begins delivering current to the battery. This current is a linearly decreasing ramp as shown in Figure 3-3d. During the time that I_2 is flowing, the battery voltage divided by the turns ratio is impressed across the primary of the choke. When I_2 ceases to flow at τ_2, the voltage across L_p drops to zero and therefore the collector voltage of Q1 drops to V_{sp}. The circuit is now ready to begin the cycle anew at time T.

3.1.2 Switching Choke Design

The first consideration in the design is the determination of the switching choke L2. Its inductance as well as its winding resistance and operating current must be determined. Before the inductance can be chosen it is necessary to know the duty factor. For reasons discussed in the duty factor modulator design section, it is necessary to keep the primary duty factor, D1, below 50 percent. The turns ratio of L2 was chosen as N = 1.5.

From the equations of Table 2-1, it is found that

$$D_1 = \frac{\sqrt{2 L_p f_s P}}{V_{sp}} \tag{3-1}$$

and

$$D_2 = \frac{\sqrt{2 L_s f_s P}}{V_B} \tag{3-2}$$

One constraint of the design is that $D_1 + D_2 \leq 1$, to permit L_s to be completely discharged during each cycle. In addition, $L_s = N^2 L_p$, which results in a solution of inductance L_p from equations 3-1 and 3-2.

$$L_p \leq 1/\left(\frac{1}{V_{sp}} + \frac{N}{V_B}\right)^2 2 f_s P \tag{3-3}$$

From equations 3-1 and 3-2 it can be seen that the duty factor will be a maximum when V_{sp} and V_B are a minimum. By substituting the values $V_{sp} = 20$ volts and $V_B = 12$ volts, $L_p \leq 32.6$ μh.

Using a value of 30 μh as a design goal, the duty factors and peak currents can be computed.

$$D_1 = \frac{5.5}{V_{sp}} \tag{3-4}$$

$$D_2 = \frac{8.22}{V_B} \tag{3-5}$$

Based on these equations, D_1 will have a range from 0.183 to 0.274, and D_2 will vary from 0.41 to 0.685.

The peak current in L_p and L_s can be found from the relationship

$$I_p(\text{peak}) = \frac{5.5}{L_p f_s} = 18.3 \text{ amps} \quad (3\text{-}6)$$

$$I_s(\text{peak}) = \frac{I_p(\text{peak})}{N} = 12.2 \text{ amps} \quad (3\text{-}7)$$

The final parameter which must be determined is the primary and secondary winding resistance for L2. If this resistance is too large then there will be excessive copper loss; however, if the resistance is specified smaller than necessary the choke will be overly large. The primary and secondary copper loss is given by the relationship

$$P_c = \frac{\left[I_p(\text{peak})\right]^2}{3} \times Rp \times D_1 + \frac{\left[I_s(\text{peak})\right]^2}{3} \times Rs \times D_2 \quad (3\text{-}8)$$

If P_c is assigned a value of 1-watt maximum, and primary and secondary losses are set equal to each other, then R_p and R_s are found to be 15 milliohms each. Table 3-2 summarizes the switching choke parameters.

Primary Inductance	30.0 μh
Secondary Inductance	67.5 μh
Turns Ratio (N)	1.5
Peak Primary Current	18.3 amps
Peak Secondary Current	12.2 amps
Primary Duty Factor Range	0.183 to 0.274
Secondary Duty Factor Range	0.410 to 0.685
Primary Resistance	15 milliohms
Secondary Resistance	15 milliohms

Table 3-2. Summary of 50-watt switching choke parameters.

3.1.3 Switching Transistor Selection (Q1)

Choice of this component must be made on the basis of four critical parameters. These are I_c(max), R_{ce}(sat), V_{CBO}, and t off.

The first parameter is the maximum collector current that the device can handle. For this design, the device must be capable of at least 18 amperes. The saturation resistance must be a minimum in order to keep the power loss to a minimum. The collector emitter breakdown voltage must be greater than $V_{sp} + V_B/N$ since this is the maximum voltage that it will see. Finally, the turn off time must be a minimum in order to minimize switching losses since the transistor sees an inductive load line at the time it turns off.

Based on these constraints, the 2N3599 was chosen. Its maximum collector current is 20 amps, R_{ce}(sat) = 0.03 ohm typically, V_{CBO} = 100 volts, and t off is typically 0.2 to 0.4 μsec.

3.1.4 Input Filter Design (L_1 - C_1)

The major consideration in the design of this filter is that

$$f_H \leq \frac{1}{2\pi} \sqrt{\frac{1}{L_1 C_1}} \leq f_s \qquad (3\text{-}9)$$

where f_H = hunting frequency

and f_s = switching frequency.

This is required so that the regulator may respond to variations in input power due to the hunting about the maximum power point, and not feed back the prime frequency rate, f_s, on the solar panel. The capacitor C1 must also be large enough so that the voltage across it does not vary greatly during each switching cycle. For these reasons C1 = 24 μf and L_1 = 1 mh were the values chosen. For these values the natural frequency for this combination is 1 khz.

3.1.5 Single Phase Duty Factor Modulator

This circuit has the function of adjusting the duty factor of the switching circuit so that the regulator operates about the solar panel maximum power point. It has four separate functional blocks and these are shown in Figure 3-4.

The 10-khz oscillator generates the clock rate for the circuit. This block is shown schematically in Figure 3-5 and it consists of Q9 through Q12 and their associated circuitry. The ramp generator develops a voltage which is proportional to time and it is synchronized by the 10-khz oscillator. This circuit consists of Q7 and Q8. The comparator compares the ramp generator output with the integrator output and generates a pulse at their zero crossover point. This circuit consists of Q3 through Q5. Finally the flip-flop Q1 and Q2 develops the final output voltage to control the switching circuit.

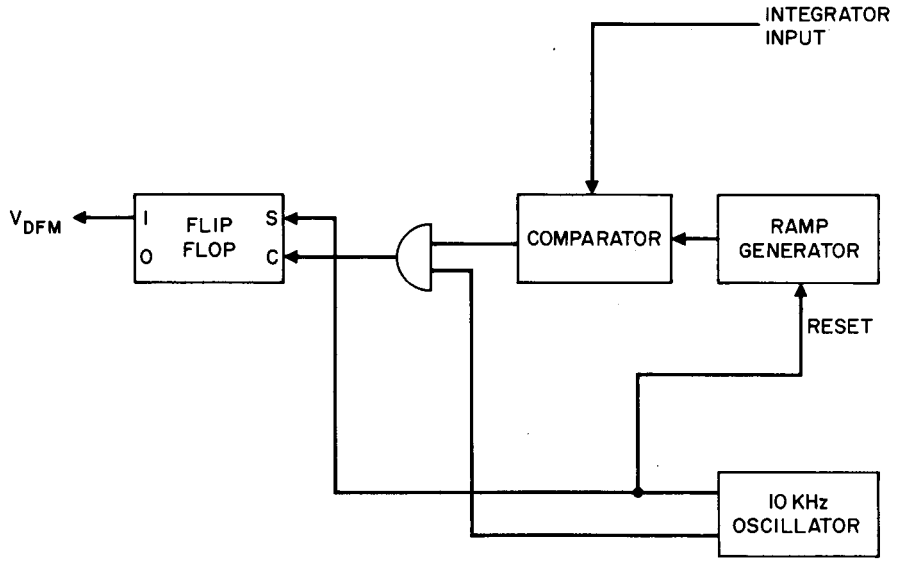


Figure 3-4. Duty factor modulator functional block diagram.

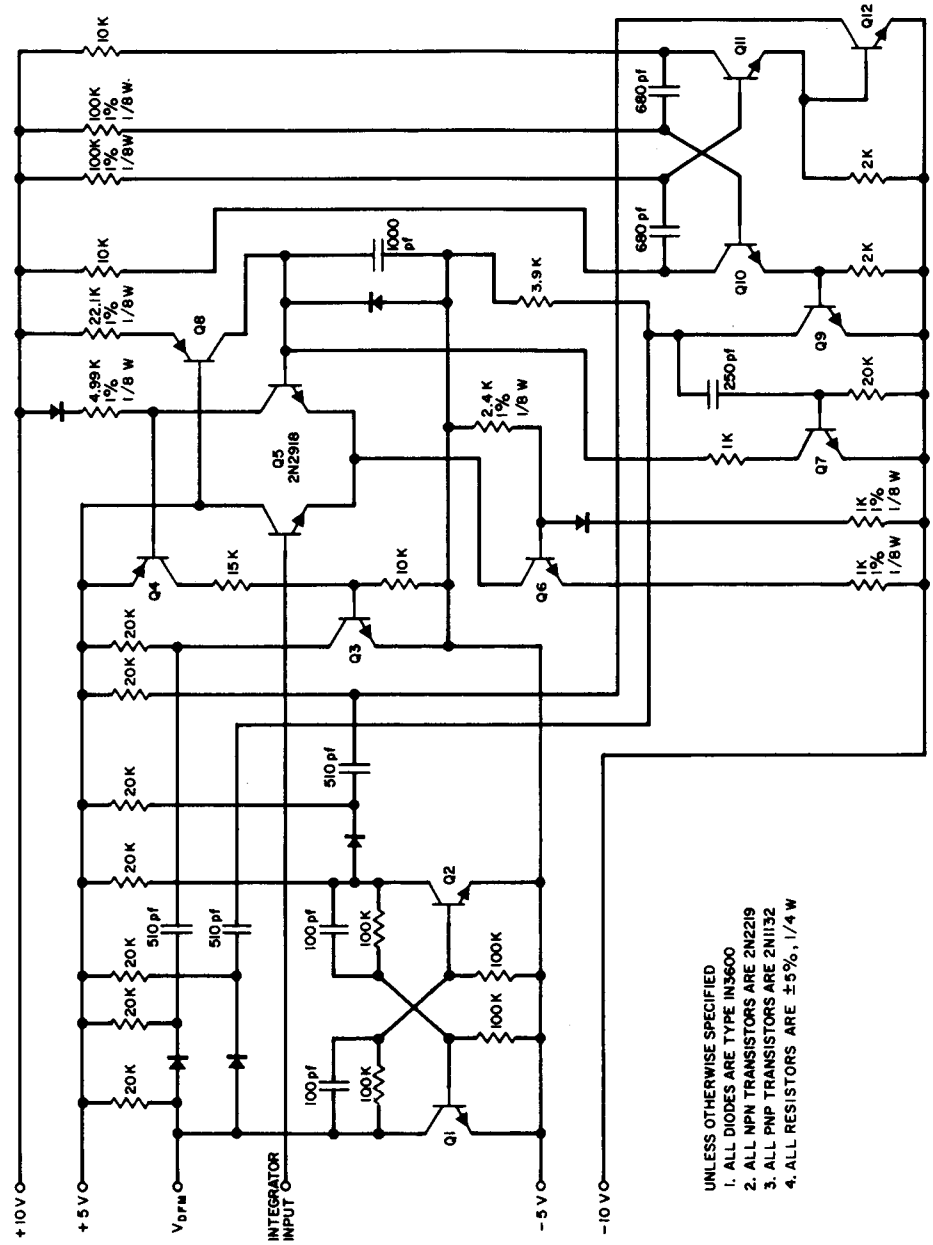


Figure 3-5. Single phase duty factor modulator schematic diagram.

If at t = 0, the oscillator output goes into its high output state, as shown in Figure 3-6a then the following two events will occur. First, the ramp generator will be reset to zero and this will allow it to begin a new cycle (see Figure 3-6b). Also, the flip-flop will be set to the high output state for V_{DFM} (Figure 3-6d). At some time τ_1 the ramp generator output voltage and the integrator input voltage will be equal. When this time occurs, the comparator will generate a pulse (Figure 3-6c). This will reset the flip-flop thereby causing V_{DFM} to go low. V_{DFM} will remain low until the beginning of the next oscillator cycle.

If the integrator input signal were not present, V_{DFM} would remain high indefinitely. To prevent this occurrence, the comparator output is combined with the inverted oscillator output and causes a pulse from the oscillator at time T/2 to reset the flip-flop. If the comparator pulse had appeared before T/2, then this pulse would have no affect. For this reason, the duty cycle can attain a maximum of only 50 percent. This prevents the main switching transistor from staying on indefinitely and shorting the solar panel.

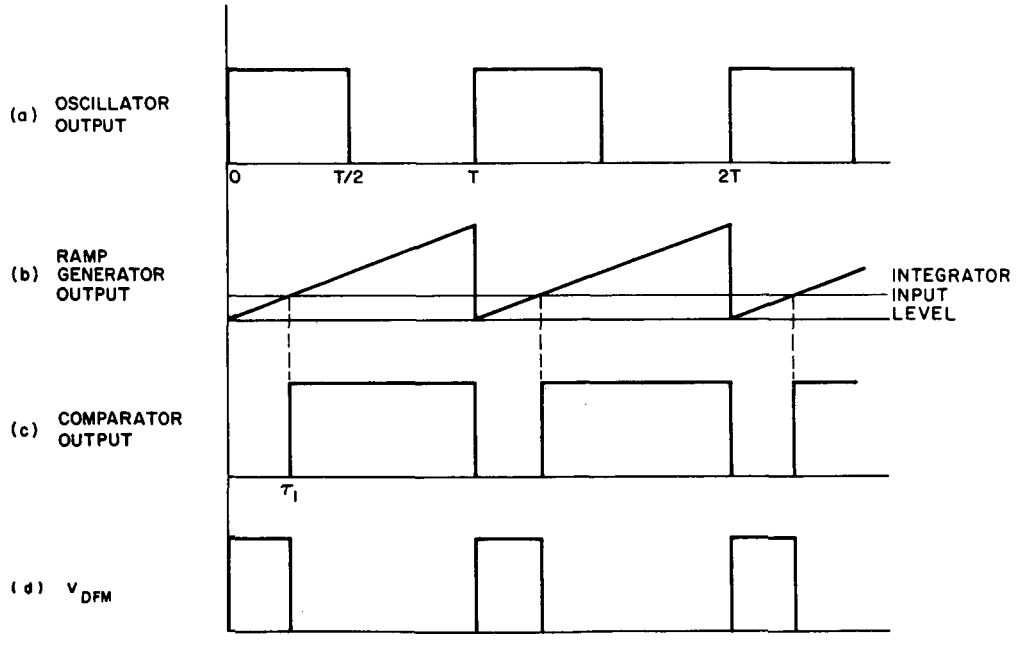


Figure 3-6. Single phase duty factor modulator waveforms.

3.1.6 Bistable and Integrator

This circuit consists of a bistable multivibrator which drives an operational amplifier with capacitive feedback. This feedback acts to integrate the bistable output. This circuit is shown in Figure 3-7. Transistors Q1 and Q2 comprise the bistable and Q3 and Q4 are the integrator.

The bistable is triggered by the pulses generated by the peak holding comparator. The resulting square wave is then integrated by the integrator, which provides the final output for this block.

The integrator output is given by the relation

$$V_o = (V_{in} / R_{in} C_1)\ t = K_1 t \qquad (3\text{-}10)$$

When Q2 is in its "off" state, the integrator input V_{in} is equal to +5 volts.

Therefore

$$K_1^+ = 5 / \left[(R_1 + R_2) \parallel R_3 \right] C_1 = 234 \text{ volts/sec} \qquad (3\text{-}11)$$

When Q2 is in its "on" state, $V_{in} = -4.3$ volts and

$$K_1^- = -4.3 / \left[R_2 \parallel R_3 \right] C_1 = -234 \text{ volts/sec} \qquad (3\text{-}12)$$

Figure 3-8 shows some of the waveforms for this circuit. The input pulses (Figure 3-8a) cause the bistable to change state thereby generating a square wave (Figure 3-8b). This square wave is then integrated to form the triangular function as shown in Figure 3-8c.

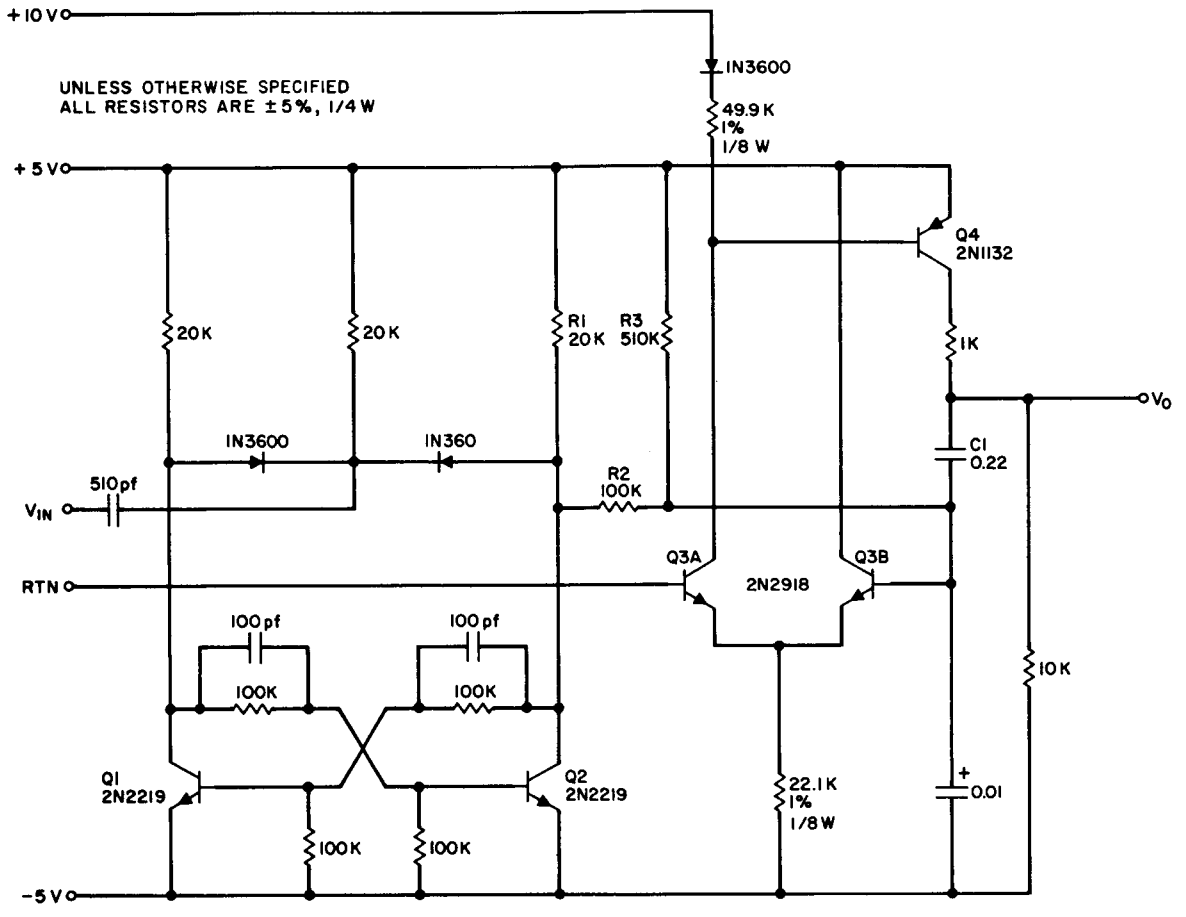


Figure 3-7. Bistable and integrator schematic diagram.

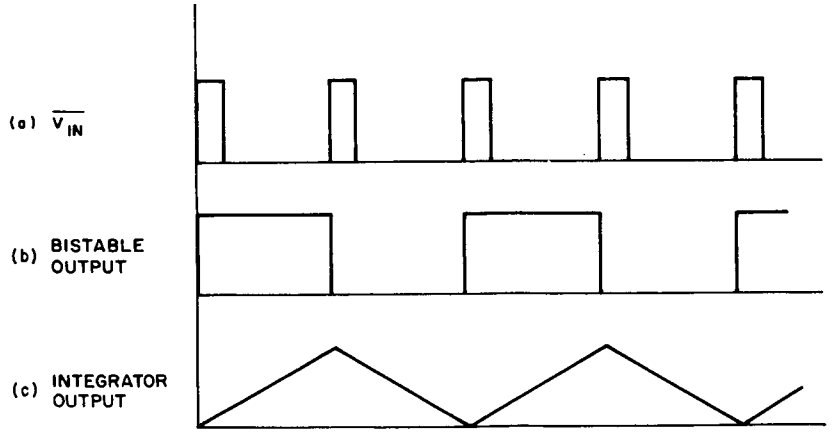


Figure 3-8. Bistable and integrator waveforms.

3.1.7 Peak Holding Comparator

This circuit acts as a memory to store a voltage proportional to the maximum current delivered to the battery. When the current drops a preset amount below the maximum point, the circuit generates a pulse which is then used to trigger the bistable.

Figure 3-9 is a schematic diagram of this circuit. The input voltage, V_{in}, is proportional to the average current delivered to the battery. As V_{in} increases, memory capacitor C1 charges through CR1

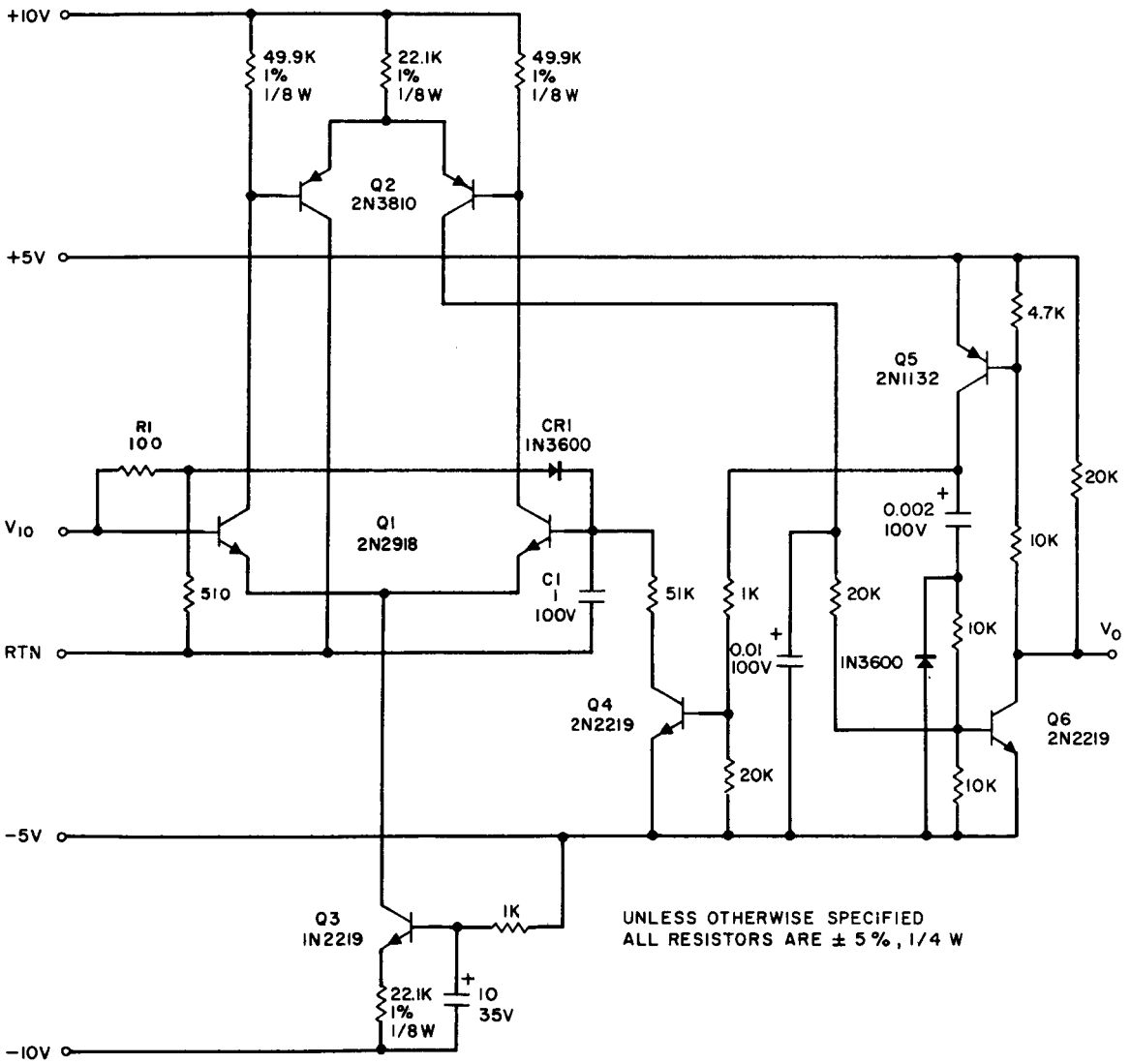


Figure 3-9. Peak holding comparator schematic diagram.

and follows V_{in}. As soon as V_{in} begins to drop, CR1 becomes reverse biased due to the charge on C1. When V_{in} has dropped a sufficient amount, the differential amplifier formed by Q1 and Q2 is unbalanced enough to cause current to flow in the collector of Q2B into the base of Q6. Transistors Q5 and Q6 form a "one-shot" multivibrator and it generates the output pulse as soon as current flows in the base of Q6. This pulse then is fed to the bistable and also back to Q4 which discharges capacitor C1. The cycle is then begun anew.

Some of the critical cricuit waveforms are shown in Figure 3-10. Figure 3-10a is a representation of the input voltage V_{in}. Two complete cycles of V_{in} represents one complete hunting cycle. The memory capacitor waveform is shown in Figure 3-10b. At the beginning of each cycle, it starts out charged to about -3 volts. It now must charge up to about +1 volt before the input voltage has reached its peak and begun to decrease. In order to do this, the current sensing amplifier which supplies the input must be capable of charging C1 through R1 as rapidly as possible. Therefore, the amplifier must be capable of supplying 30 to 40 ma in surges. The waveform in Figure 3-10c illustrates the output pulses which are generated by the "one-shot".

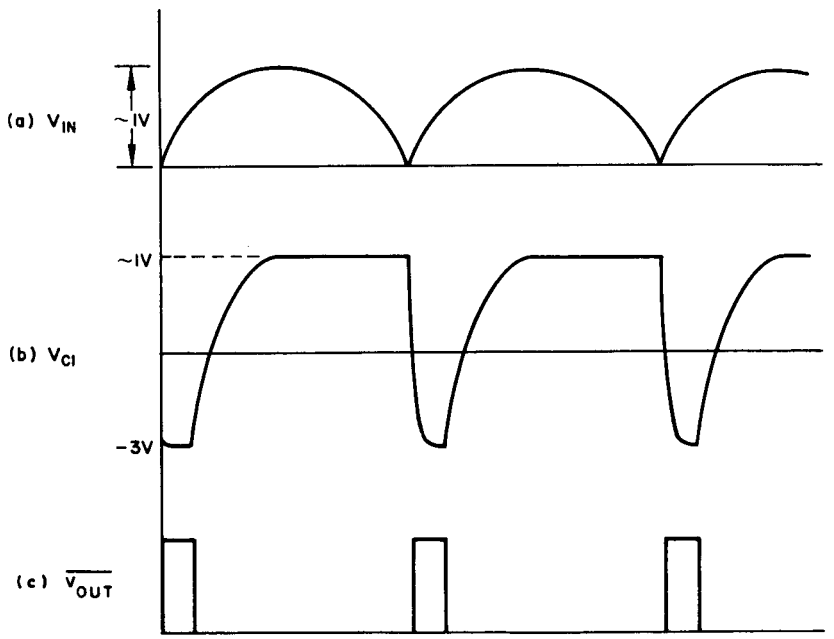


Figure 3-10. Peak holding comparator waveforms.

3.1.8 Current Sensing Amplifier

This circuit amplifies the voltage developed across the sensing resistor R_s, and raises it to a level which is usable by the peak holding comparator. From the standpoint of efficiency, the current sensing resistor must be as small as possible since it represents a resistance in series with the battery current. However, the smaller the sensing resistor the higher the gain of the sensing amplifier must be since the voltage to trigger the peak holding comparator (ΔV) is fixed at about 1 volt.

In order to keep the hunting losses below 1 watt, the peak-to-peak current change (ΔI_B) at the hunting frequency was chosen to be 100 ma. The determination of the hunting losses is based on the assumption that

$$P_{(hunting)} = \Delta I_B(avg)\, V_B = \frac{\Delta I_B\, V_B}{2} \qquad (3\text{-}13)$$

Therefore the amplifier gain at this frequency can be determined from the following relationship

$$A = \Delta V/\Delta I_B \times R_s = 300 \qquad (3\text{-}14)$$

A schematic diagram of this unit is shown in Figure 3-11. Transistor Q1 provides a differential input and then this is followed by three stages of gain in order to provide the necessary 30 to 40 milliamps of surge current required by the peak holding comparator. The amplifier has a feedback loop which sets the gain to the desired amount.

The gain characteristic of the amplifier is determined by the internal gain stabilization networks plus the feedback networks. Since a single RC cut network will provide 20 db/decade of attenuation, three of these gain cuts are provided in order to insure that the switching frequency component of the battery current will be sufficiently attenuated so as not to affect the peak holding comparator. A plot of gain in db versus natural frequency is shown in Figure 3-12.

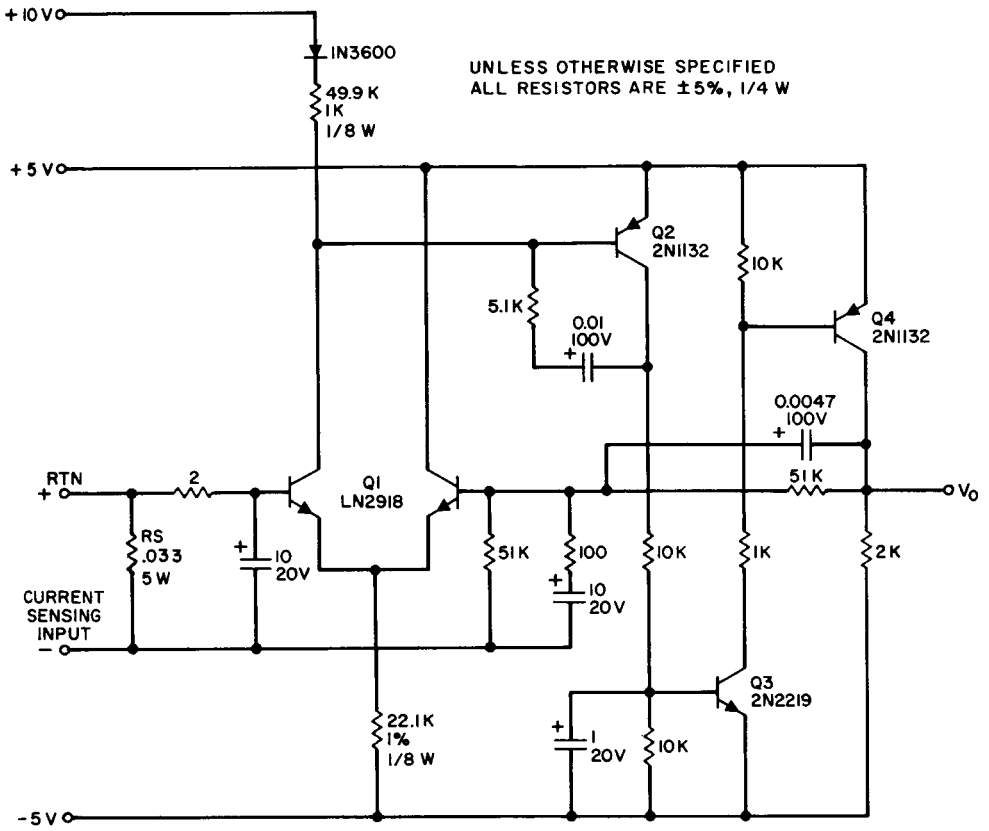
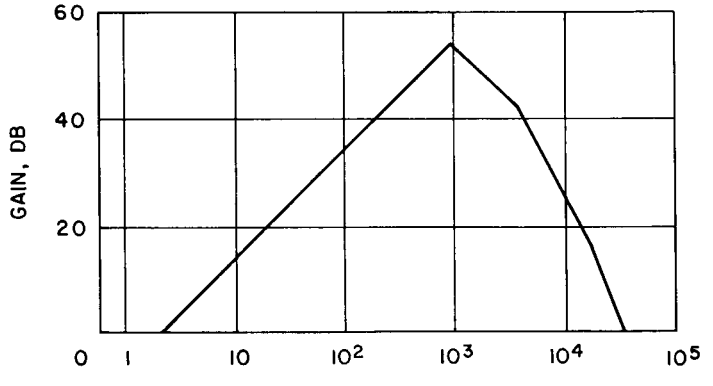


Figure 3-11. Current sensing amplifier schematic diagram.



$$\text{GAIN} = \frac{(JW/2+1)}{(JW/10^3+1)^2\,(JW/4\times10^3+1)\,(JW/20\times10^3+1)}$$

Figure 3-12. Current sensing amplifier frequency response curve.

3.1.9 Non-Optimum Controller — Trickle Charge Regulator

In order to provide an alternate low power charging mode once the battery has achieved full charge, a trickle charge controller is provided. This circuit senses the average current flowing into the battery and then adjusts the duty factor modulator in such a manner as to cause the battery current to be a low constant value.

Figure 3-13 is a schematic diagram of this circuit. It consists of two basic functional blocks. The first is a low pass amplifier which raises the millivolt signal developed across the current sensing resistor to a usable level. This amplifier is composed of transistors Q1 through Q5. The second portion of the circuit is a comparator which compares the amplifier output to a reference voltage. The output of the comparator adjusts the slope of the ramp generator in the duty factor modulator.

Modification of the slope of the ramp causes the duty factor to be changed, thereby adjusting the battery current. This circuit consists of Q6 through Q10.

A charge mode control circuit is also provided for the 50-watt regulator. This circuit senses the battery voltage and when it reaches 20 volts it automatically commands the regulator into the trickle charge mode. The regulator remains in this mode until the battery voltage drops below 18 volts. Figure 3-14 is a schematic diagram of the charge mode control. The output, V_o, is applied to the base of Q11 of Figure 3-13. During optimum charging operation, Q3 has no base drive which inhibits the trickle charge regulator. When the voltage has risen to the required amount, Q3 turns "on" thereby enabling the trickle charger.

3.1.10 Switching Regulator and Bias Converter

The final block which must be considered in the design of the OCR is the switching regulator and bias converter. In order to provide the regulated ±5 volts and ±10 volts for the biasing of all the circuitry, a bias converter is provided to generate these voltages. Regulation is obtained by a switching mode voltage regulator which supplies the input to the converter. The regulator senses the +5-volt converter output and

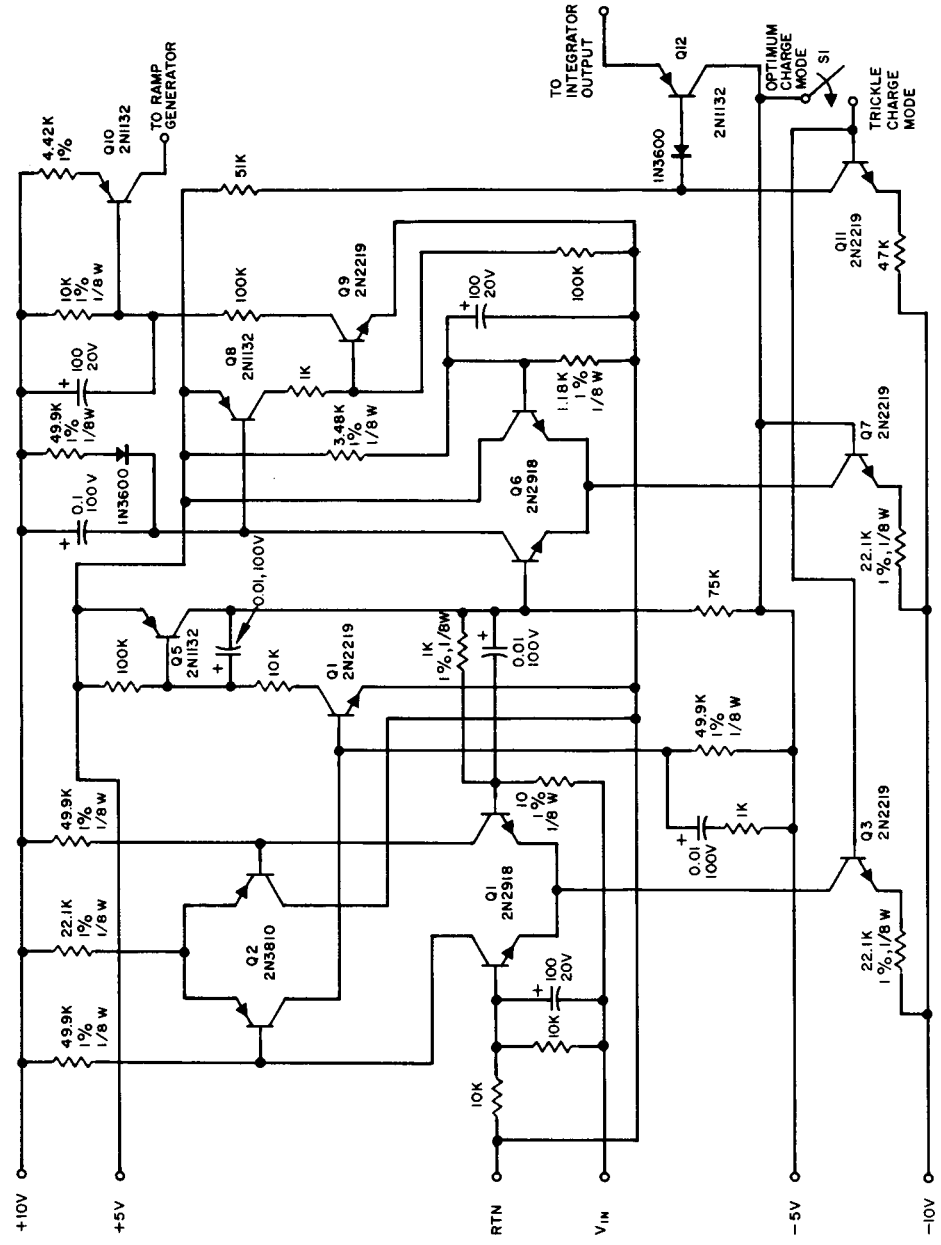


Figure 3-13. Non-optimum controller - trickle charge regulator.

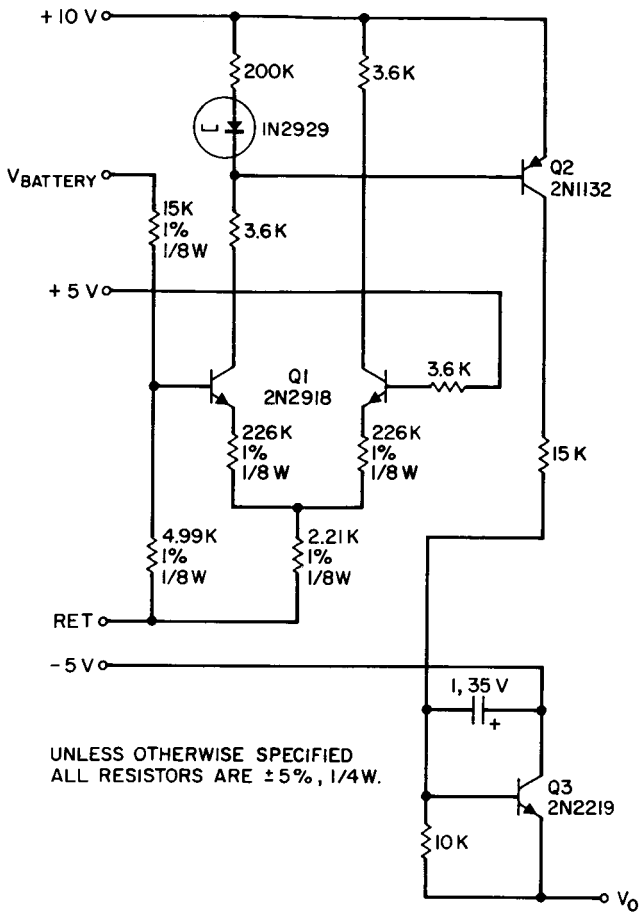


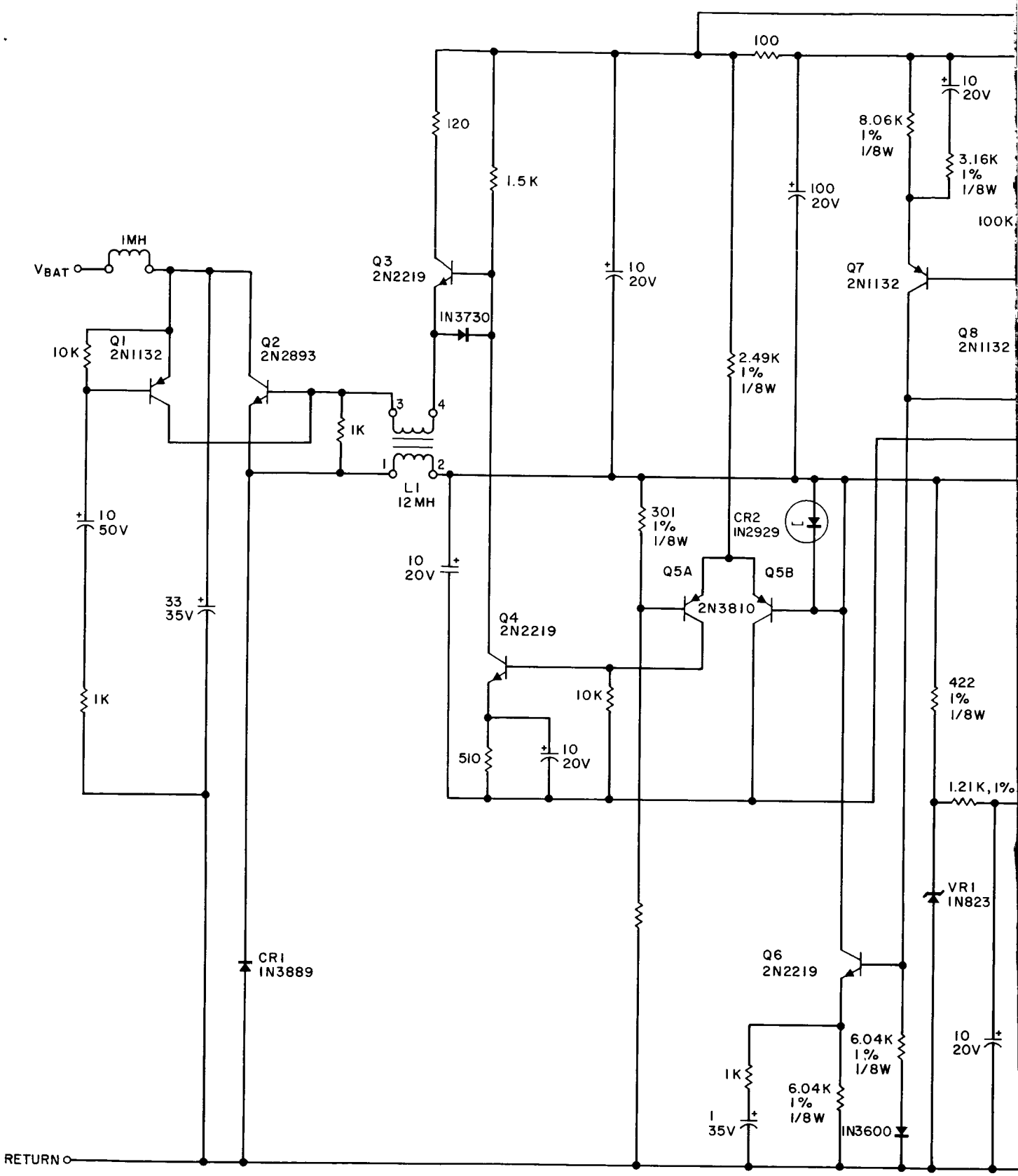
Figure 3-14. Charge mode control schematic diagram.

uses it to control its d-c output voltage. While the switching regulator is more complex than a comparable linear regulator, its efficiency is considerably higher over the entire expected input voltage range. Efficiencies of 80 to 90 percent are possible at the low power level, which this regulator operates.

Figure 3-15 is a schematic diagram of this circuit. Transistors Q2 through Q9 comprise the switching regulator and Q10 and Q11 are the bias converter. Transistor Q1 acts as a starter for the regulator as it is not self-starting.

The bias converter is a square loop oscillator which depends on the saturation of the core of transformer T1 to cause switching to take place. The resulting square wave is transformed, rectified, and filtered to provide the necessary bias voltages.

Operation of the switching regulator can be described using the block diagram of Figure 3-16. If at time $t = 0$, the main switch Q2 is "on", then V_o will be rising; its rate of rise limited by L1 and C1.



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(1)

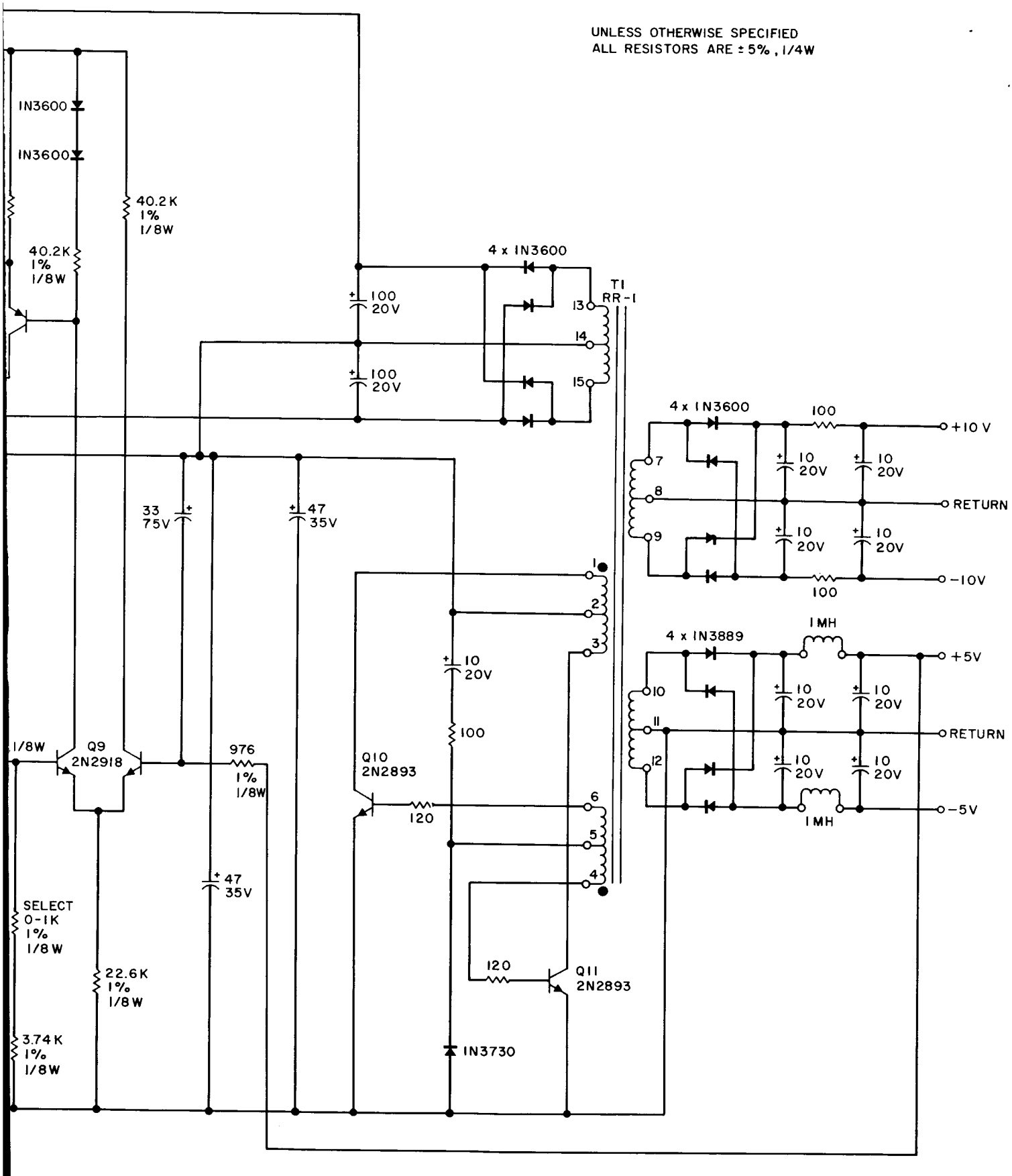

Figure 3-15. Switching regulator and bias converter.

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3-20-1

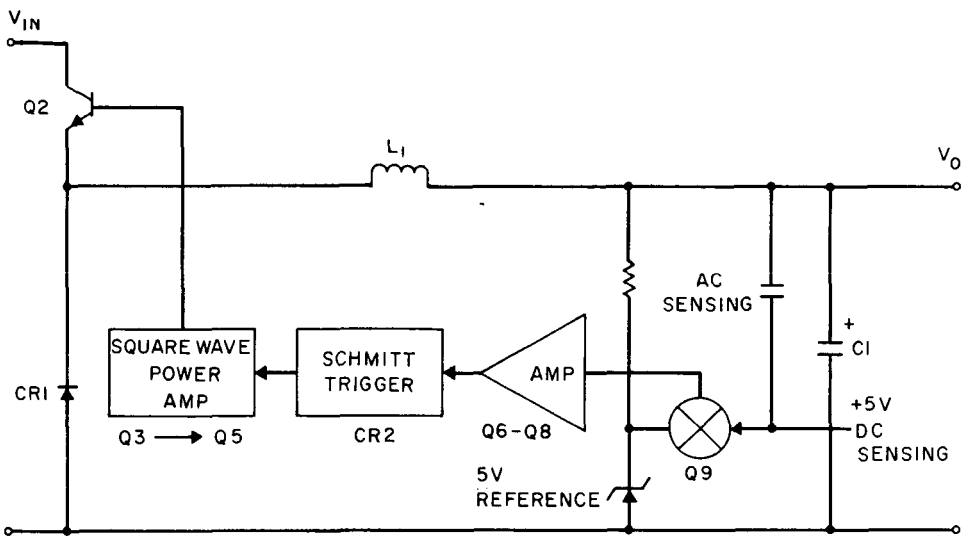


Figure 3-16. Switching regulator functional block diagram.

The difference between V_o and the reference voltage is amplified. When the amplifier output reaches a predetermined level, it causes the Schmitt trigger to reverse state. This reversal is amplified by the power amplifier and causes Q2 to turn "off". With Q2 "off", the output voltage begins decreasing. When it reaches a predetermined lower level the Schmitt trigger reverts to its original state and Q2 turns "on". At this time the cycle begins again. Because of the high gain of the amplifier, the Schmitt trigger firing levels may be maintained within millivolts of the average d-c output voltage.

Both AC and DC sensing are provided to control the regulator. DC sensing of the +5-volt converter output causes the regulator output to adjust its d-c output, V_o, to whatever is necessary to maintain the bias at +5 volts. AC sensing is provided directly from the regulator output bus to prevent converter noise from affecting the regulator switching operation.

3.2 CASE II: 250-WATT REGULATOR DESIGN

Functionally this circuit is identical to that described in the 50-watt regulator discussion. It has the same block diagram as shown in Figure 3-1 except that a charge mode control is not provided for this case, since its operation does not have to be completely automatic.

Table 3-1 summarizes the specifications for this unit. Because of the high power involved, the switching frequency was chosen to be 2 khz. In order to insure that the hunting frequency was well below this value, a range of 20 to 60 hz was chosen.

3.2.1 Switching Circuit

Basically, this circuit is identical to the 50-watt switching circuit except that it is a two phase circuit. All this means is that two identical single phase circuits are utilized and each circuit operates in the manner described for the 50-watt case.

Figure 3-17 is a schematic diagram of the switching circuit. All of the major parameters can be determined as previously described. Table 3-3 summarizes the switching choke parameters (L1 and L2).

Selection of the main switching transistors, Q1 through Q4, was made using the same criteria as before. However, since the device chosen has a V_{CBO} of 100 volts, the turns ratio of the switching choke was chosen to be two in order to limit the maximum collector voltage to 70 volts. Also for this case, two of these devices were paralleled in order to reduce the saturation losses.

The input filter was chosen to have a natural frequency of about 300 hz in order to meet the criteria of equation 3-9.

3.2.2 Two-Phase Duty Factor Modulator

The function of this circuit is similar to that of the single phase circuit. Additionally, it must generate two outputs which are 180 degrees out of phase. The primary problem is the requirement that both outputs have exactly the same duty factor. It is of prime importance to insure that there will be no duty factor unbalance between the two phases of the switching circuit or a power loss will occur.

Figure 3-18 is a block diagram of a two phase duty factor modulator. It contains a 4-khz oscillator, a ramp generator, a comparator, and four flip-flops. The waveform shown in Figure 3-19a is the oscillator reference frequency which is twice the prime switching rate of 2 khz. The ramp generator is synchronized by the clock and produces

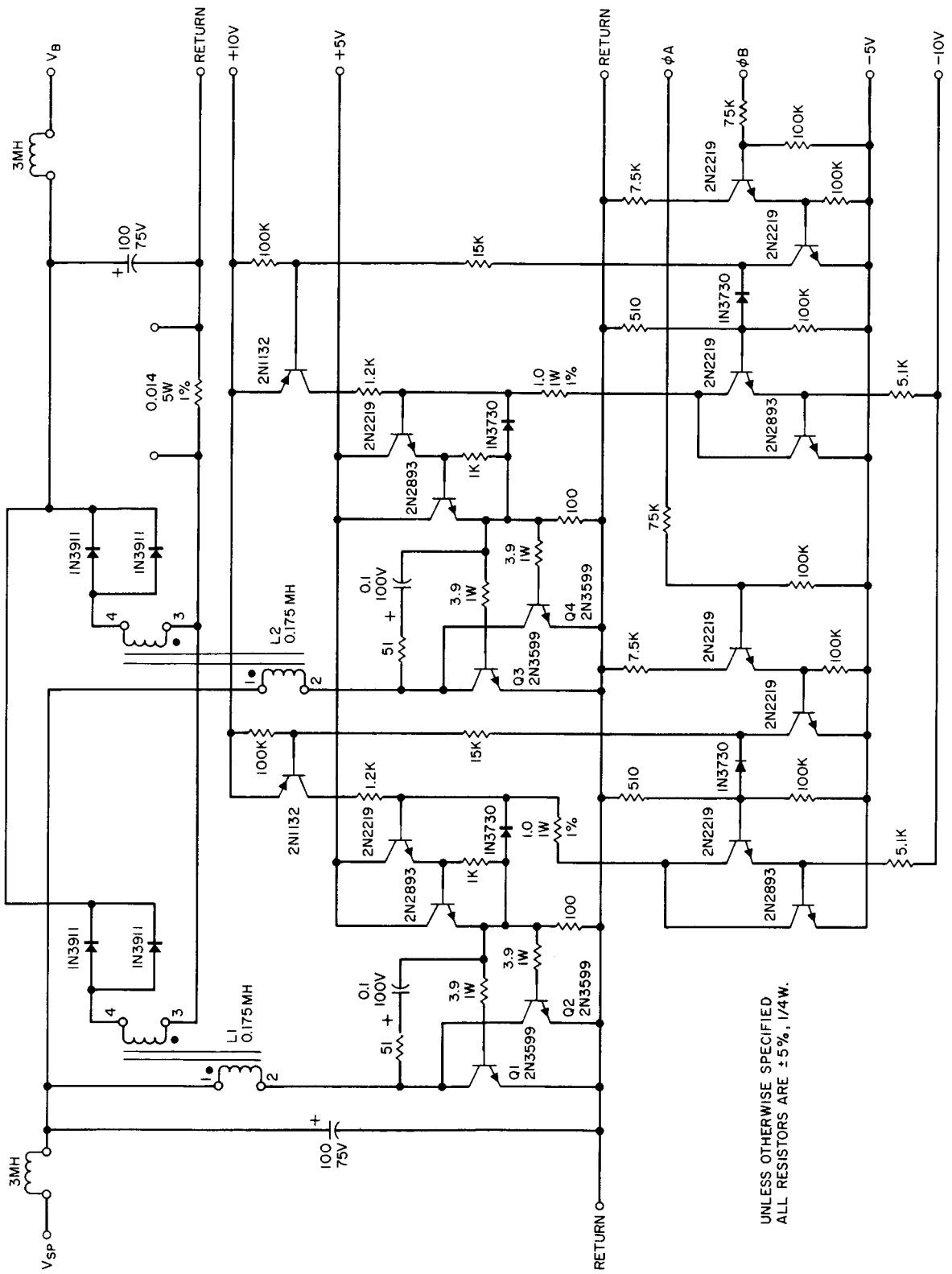


Figure 3-17. 250-watt optimum charge regulator 2ϕ switching circuit.

Choke Parameters	Measured Value
Primary Inductance	170 uh
Secondary Inductance	680 uh
Turns Ratio (N)	2
Peak Primary Current	27 amps
Peak Secondary Current	13.5 amps
Primary Duty Factor	0.184 to 0.23
Secondary Duty Factor	0.46 to 0.736
Primary Resistance	15 milliohms
Secondary Resistance	15 milliohms

Table 3-3. Summary of 250-watt switching choke parameters.

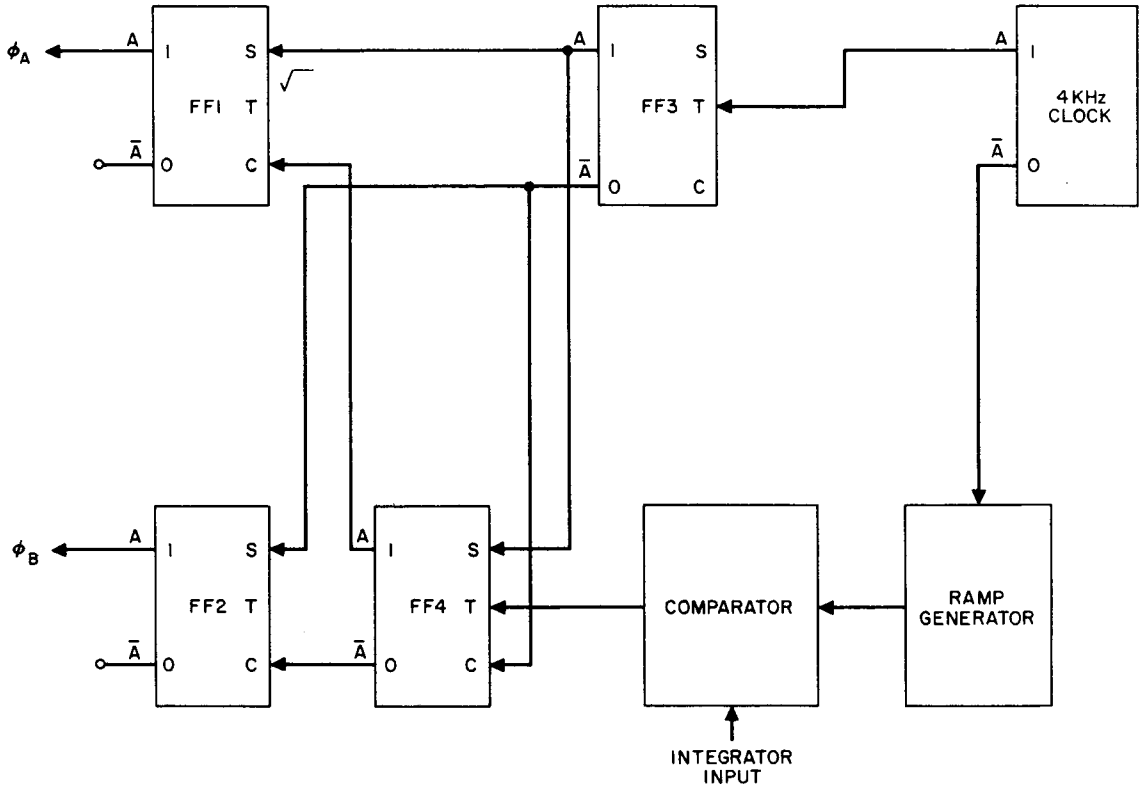


Figure 3-18. Two phase duty factor modulator.

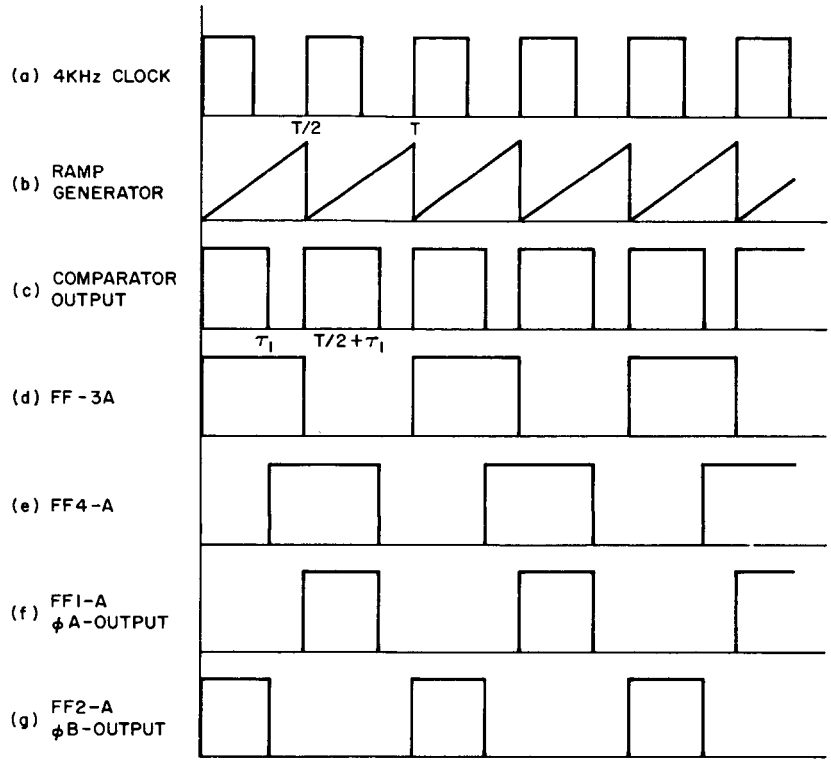


Figure 3-19. Two phase duty factor modulator waveforms.

a voltage ramp each clock cycle. This amouts to two identical voltage ramps each switching cycle (Figure 3-19b). Since each cycle is identical, the comparator produces two pulses each switching cycle of exactly the same duration. The first pulse is used to control the duty factor of one phase and the second to control that of the second phase (Figure 3-19c).

The clock output is also used to drive FF-3 at one half of the clock rate, thereby generating the prime switching frequency (Figure 3-19d). Each time FF-3 switches it causes either FF-1A or FF-2A to go into its high state, which turns "on" the main switching transistor.

The comparator output is used to drive FF-4. It is also driven at one half the clock rate but its switching times are shifted a fixed time, τ_1 , from the time FF-3 switches (Figure 3-19e). Each time FF-4 switches it causes either FF1-A or FF-2A to revert to its low state.

Synchronization pulses are also provided from FF-3 to FF-4 so as to insure the proper phasing between the two. These pulses also insure that a maximum duty cycle of 50 percent is never exceeded when the comparator output is not present. Figures 3-19f and g show the final DFM output waveforms for phases A and B.

Figure 3-20 is a schematic diagram of this circuit. Transistors Q1 through Q8 comprise the four flip-flops. They are all of similar construction and they are triggered by negative going pulses. Transistors Q9 through Q12 make up the comparator, Q13 and Q14 is the ramp generator, and Q15 through Q18 is the clock.

3.2.3 Other Circuits

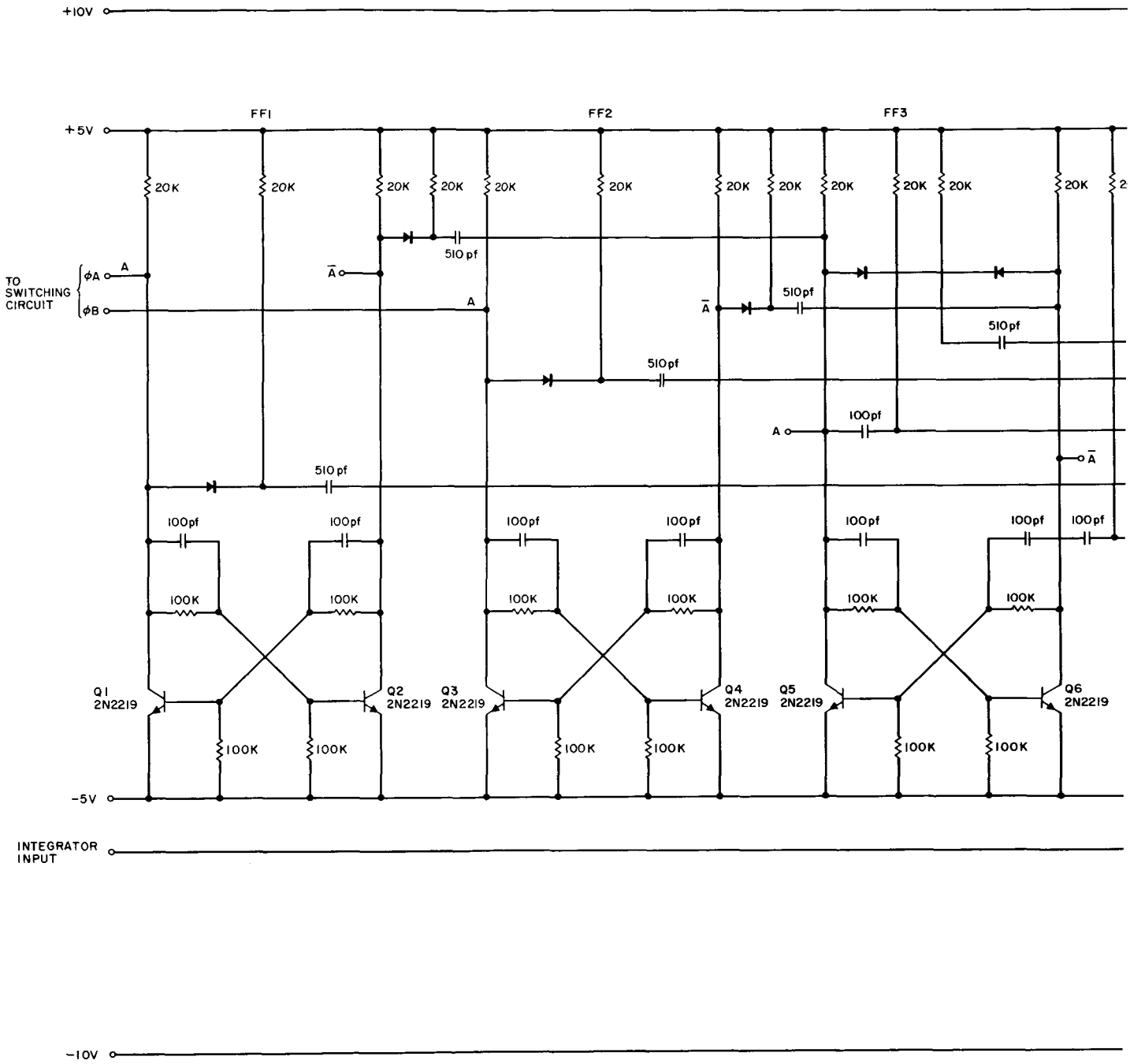
The balance of the circuits are identical to the ones described for the 50-watt regulator. The only component differences exist in the amplifier, where the gain cut and compensation networks are modified so as to effectively filter the 2-khz switching frequency. The only other difference is the size of the integrator feedback capacitor, since this unit hunts at about one-fifth the rate of the 50-watt unit.

3.3 COMPONENT SELECTION

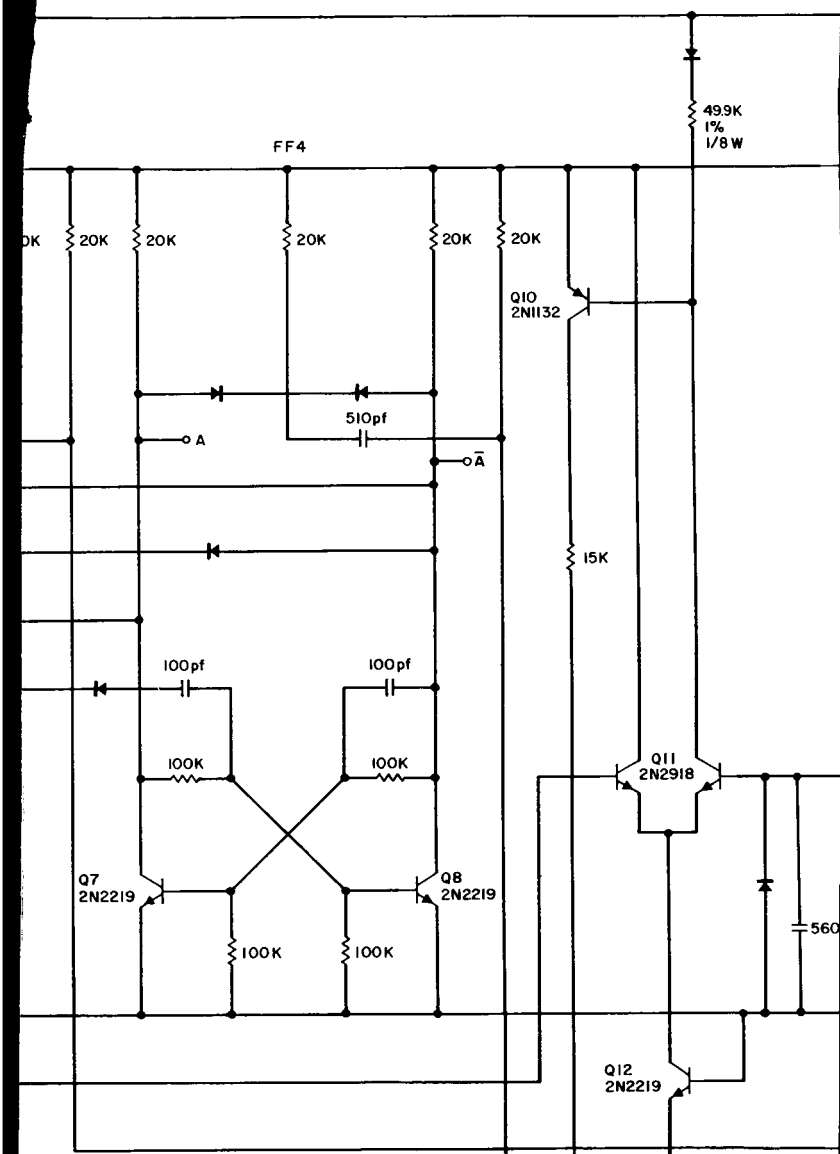
In general most of the semiconductors selected for use in the design of the regulators are space or military qualified devices although commercial equivalents are used in the breadboard construction. In two specific cases the device is being qualified and is used in active Hughes programs.

Table 3-4 is a list of the semiconductor parts used. It shows commercial part numbers and also shows applicable military and/or Hughes part numbers. In most cases these Hughes numbers represent Syncom or Surveyor specifications.

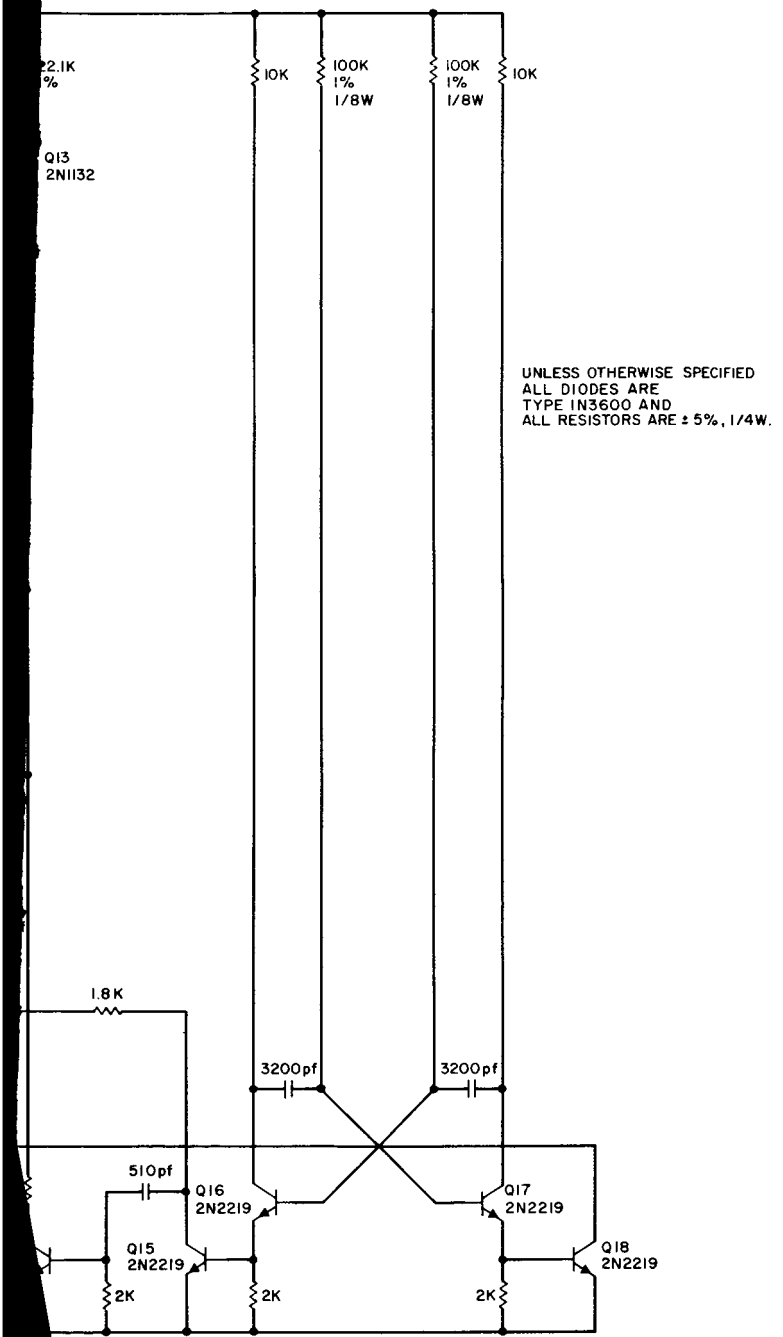
All of the filter chokes were purchased from Magnetic Circuit Elements, Inc. of Montrose, California. The switching chokes were designed by the Hughes Components Department and specifications for their design exist under the part numbers given in the ABM. Figures 3-21 and 3-22 show winding information for the bias converter transformers.


+10V
FF1
FF2
FF3
+5V
20K
510 pf
TO SWITCHING CIRCUIT
φA
φB
A
Ā
100pf
100K
Q1 2N2219
Q2 2N2219
Q3 2N2219
Q4 2N2219
Q5 2N2219
Q6 2N2219
-5V
INTEGRATOR INPUT
-10V

3-27-1


FF4
49.9K
1%
1/8W
20K
20K
20K
20K
20K
Q10
2N1132
510pf
A
Ā
15K
100pf
100pf
100K
100K
Q11
2N2918
Q7
2N2219
Q8
2N2219
100K
100K
560
Q12
2N2219
Q9
2N2219
2K
22.1K
1%
1/8W

3-27-(1)



ıre 3-20. Two phase duty factor modulator schematic diagram.

Commercial Part Number	Manufacturer	Description	Military or Hughes Part Number
2N3599	Solatron	20 amp power	988846-2
2N2893	Fairchild	3 amp power	988850-4
2N2219	Motorola	TO-5 npn	988836-1/ USA 2N2219
2N1132	Motorola	TO-5 pnp	988843-1/ USN 2N1132
2N2918	Fairchild	npn matched pair	988863-3
2N3810	Motorola	pnp matched pair	928263-3
1N3911	T.I.	30A power diode	Being qualified
1N3910	T.I.	30A power diode	Being qualified
1N3889	T.I.	6A power diode	988751-1
1N3730	Raytheon	Glass pkg diode	988743-1
1N3600	Fairchild	Glass pkg diode	988740-1/ USN 1N3600
1N2929	Hoffman	1 ma tunnel diode	988712-12
1N823	Motorola	6.2 V zener diode	988706-2

Table 3-4. Summary of semiconductor types used.

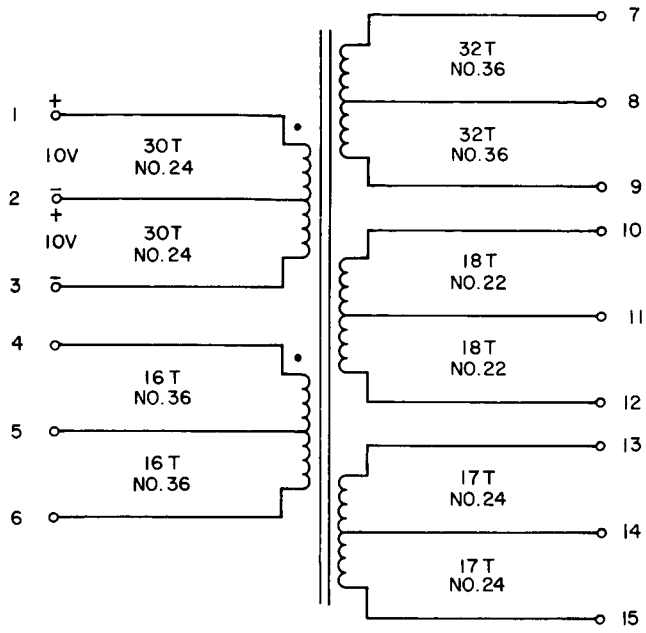


Figure 3-21. 50-watt regulator — bias converter transformer RR-1.

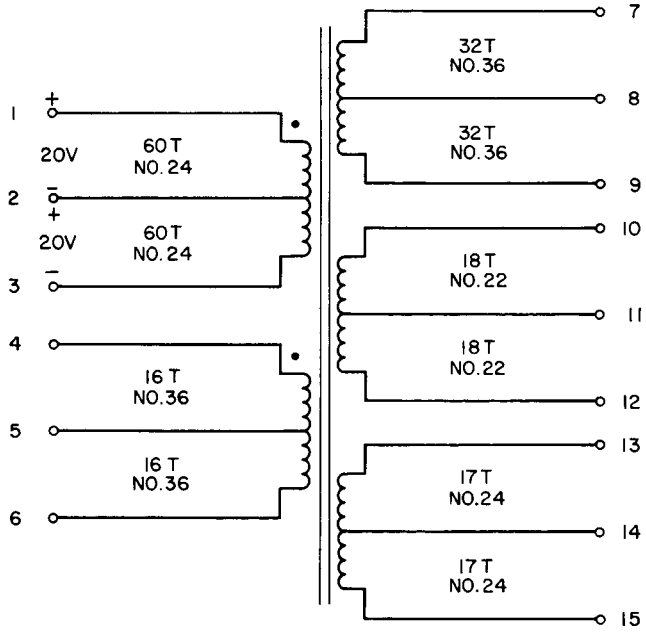


Figure 3-22. 250-watt regulator — bias converter transformer RR-2.

4. EVALUATION OF GENERAL CIRCUIT OPERATION

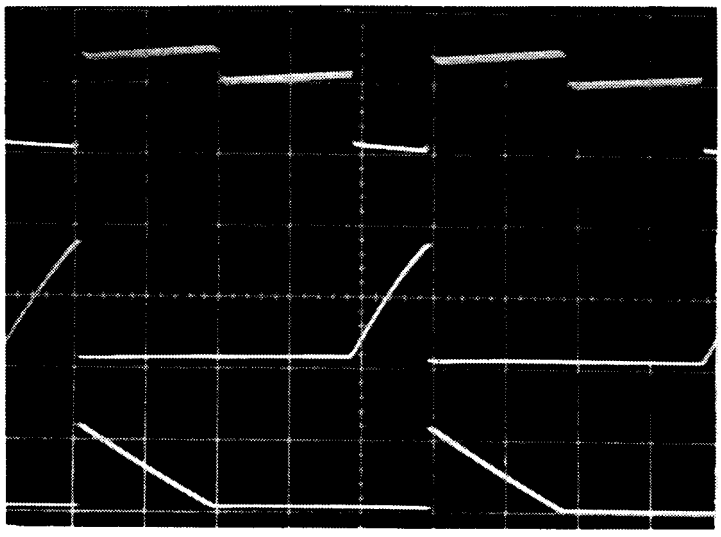
In general, circuit operation of the 50-watt and the 250-watt regulators was evaluated and found to be satisfactory over the entire range of expected solar panel, battery, and environmental variations. Tests were run at room temperature as well as at -40°C and +70°C and no adverse effects were seen due to this variation. Operation of the 50-watt regulator during the 30-percent power transient was also satisfactory. The efficiency goals of 80 and 90 percent were not met for the 50 and 250-watt regulators, respectively. Further discussion on how these goals may be approached more closely is contained in this section.

4.1 50-WATT REGULATOR EVALUATION

The operation of this unit was satisfactory in all respects. The unit exhibited stability of operation for all conditions including the -30 percent power transient.

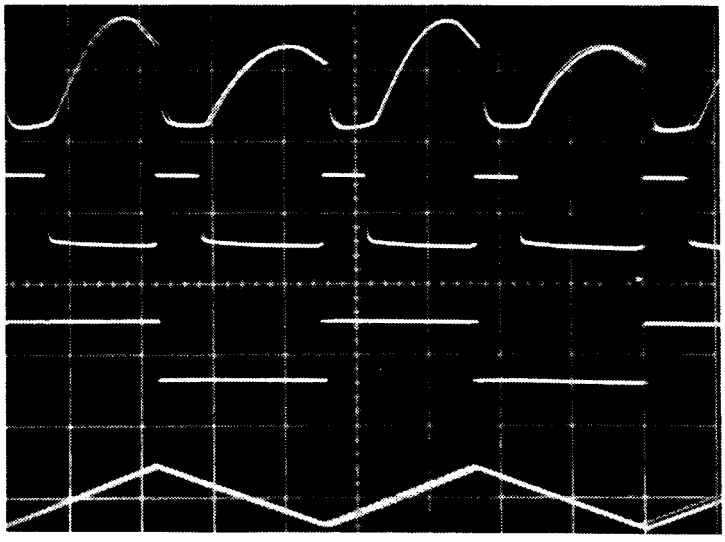
The circuit operation was very close to that which was theoretically predicted. The following figures are oscilloscope photographs taken of the actual circuit waveforms. From these oscillograms many of the operating parameters may be determined.

Figure 4-1 is a photo of the switching circuit waveforms. As seen in the photo, the switching frequency is 10 khz and the duty factor averages about 0.21. This is well within the predicted range of 0.183 to 0.274 (see Section 3.1.2, Table 3-2). The peak primary and secondary currents as seen in this photo, are about 18 and 12 amperes, respectively. The predicted values are also shown in Table 3-2. The final information that can be obtained from this photo is the maximum voltage seen by the main switching transistor, Q1. It appears to be 30 volts, but what is not shown is the fact that a voltage spike exists at the time Q1 turns "off" (t = 2.0 μsec). This spike can be seen in Figure 4-6 and it shows the maximum collector voltage of Q1 to be 60 volts. This is still safely below the maximum V_{CBO} for the device.



(a) V_{ce} (Q1) - Vertical:20V/cm
(b) I_1 - Vertical:10A/cm
(c) I_2 - Vertical:10A/cm
} horizontal:20 μsec/cm

Figure 4-1. 50-watt OCR switching circuit waveforms. (See Figure 3-3.)



(a) Current Sensing Amplifier Output - Vertical:5V/cm
(b) Peak Holding Comparator Output - Vertical:10V/cm
(c) Bistable Output - Vertical:10V/cm
(d) Integrator Output - Vertical:0.5V/cm
} horizontal: 1msec/cm

Figure 4-2. 50-watt OCR control loop waveforms. (See Figure 3-8 and 3-10.)

Stability of operation can be seen from observing the control loop waveforms. Figure 4-2 shows some of these. As seen in the photo, there is very little waveform jitter, which indicates stable operation in the hunting zone. Figure 4-2a shows the output of the current sensing amplifier. In addition, this is the input to the peak holding comparator (PHC) and it can be seen that a ΔV of about 1 to 2 volts is required to cause an output pulse from the PHC (Figure 4-2b). The output waveform for the bistable is shown in Figure 4-2c, and it indicates the hunting frequency is 220 hz.

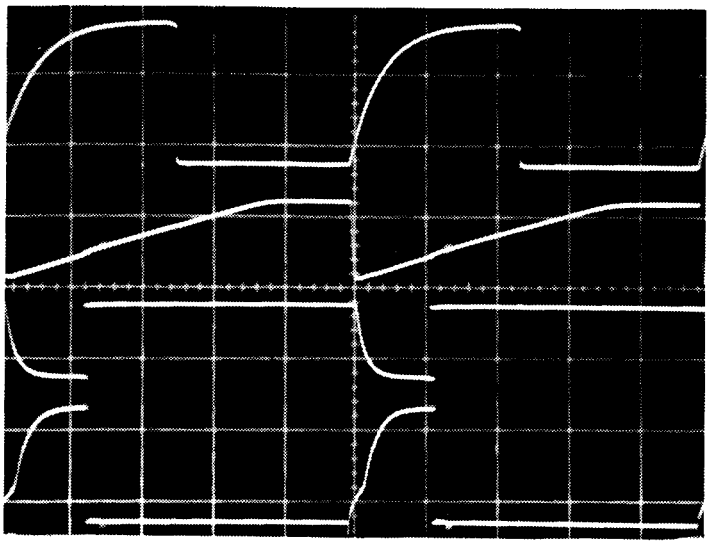
In order to verify this result, the hunting frequency can be calculated using equation 2-19. If the design values listed in Table 4-1 are substituted into the equation a value of 212 hz is obtained for f_H. Using the measured values, it is found that f_H = 243 hz. The design value is about 5 percent below the measured value and this is within the design accuracy.

The last waveform of Figure 4-2 is the integrator output voltage, which is useful in determining the integrator constant K_1. For a positive going voltage, it is 250 volts per second and for the negative going voltage, it is 208 volts per second. If an average of the two is taken then K_1 = 229 volts per second. In order to determine the constant, K, associated with ΔD_1, it is necessary to examine the duty factor modulator ramp generator waveform. This waveform is shown in Figure 4-3b. The slope of this ramp is 15 volts per 100 μsec switching period. Therefore, it is found that $K = K_1/15$ or 15.3 volts per second per volt.

Figure 4-3 also shows some of the other duty factor modulator waveforms and their relationship to each other. These waveforms may be compared to those predicted in Section 3.1.5, Figure 3-6. It may be noted that the ramp generator output (Figure 4-3b) saturates about 70 percent of the way through the cycle. This is done purposely to increase the sensitivity of the DFM comparator by making the effective peak-to-peak output of the ramp generator greater than the 10-volt supply voltage. The slope of the ramp could be increased until the generator saturated at 50 percent without affecting circuit operation. This is true since the duty cycle of the switching circuit has a 50-percent maximum.

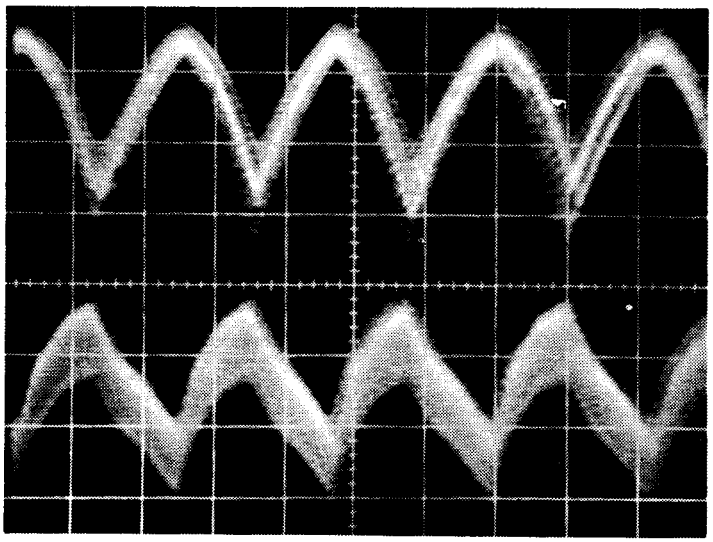
Parameter	Design Value	How Determined	Measured Value	How Determined
Efficiency	0.8	Design Goal	0.76	$P_{out}/P_{in} + P_{hunting}$
Solar Panel Voltage - V_{sp}	25 volts	Nominal Design Value	26 volts	DC Measurement
Battery Voltage - V_B	20 volts	Nominal Design Value	20 volts	DC Measurement
Solar Panel Voltage Change - ΔV_{sp}	1.4 volts	$\Delta V_{sp} = \frac{\sqrt{2L_p f_s P}}{V_{sp}} \Delta D_1$	1.25 volts	Figure 4-4
Primary Duty Factor	0.22	$D_1 = \frac{\sqrt{2L_p f_s P}}{V_{sp}}$	0.21	Figure 4-1
Battery Current Change - ΔI_B	0.1 amp	Nominal Design Value	0.1 amp	AC Measurement
Integrator Constant	15/sec	Nominal Design Value	15.3/sec	Figure 4-2d and Figure 4-3b
Choke Primary Inductance	30 uh	Nominal Design Value	30 uh	- - - - - - - - -
Switching Frequency	10 khz	Nominal Design Value	10 khz	Figure 4-3a

Table 4-1. Summary of circuit parameters for hunting frequency determination, 50-watt OCR.



(a) Clock Output - Vertical:10V/cm
(b) Ramp Generator Output - Vertical:10V/cm
(c) Comparator Output - Vertical:10V/cm
(d) Flip-Flop Output (V_{DFM}) - Vertical:5V/cm
} horizontal: 20 μsec/cm

Figure 4-3. 50-watt OCR duty factor modulator waveforms. (See Figure 3-6)



(a) V_{sp} - Vertical:1 volt/cm
(b) I_{sp} - Vertical:100 MA/cm
} horizontal:2msec/cm

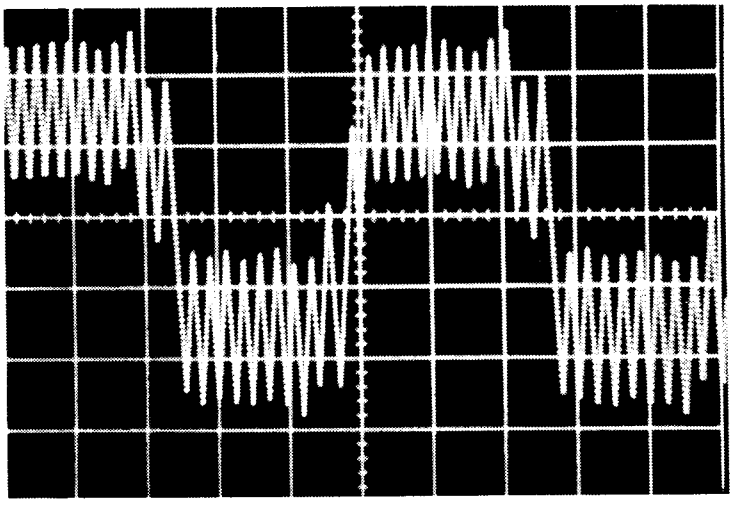
Figure 4-4. 50-watt OCR solar panel AC output voltage and current.

A measurement of the solar panel voltage change during each cycle may be seen in Figure 4-4. The peak-to-peak change each cycle is 2.5 volts. Assuming symmetry of each half cycle the change in voltage V_{sp}, from P_{mp} to P_2 will be 1.25 volts. In order to verify this result V_{sp} can be calculated from the following equation.

$$\Delta V_{sp} = -\frac{\sqrt{2L_p f_s P}}{D_1^2} \Delta D_1 \qquad (4\text{-}1)$$

ΔD_1 is found to be -0.0125 and therefore, ΔV_{sp} = 1.4 volts.

Of final consideration is the stability of this unit during the -30 percent power transient. To simulate this transient, a 10-hz square wave with 15 msec rise and fall times modulated the solar panel illumination characteristic to cause it to change ±15 percent about its nominal value. The affect of this modulation can be seen in the integrator output waveform which is shown in Figure 4-5. As shown, stable operation is provided by the integrator shifting its operating point to account for the power change.



Vertical:2 V/cm; Horizontal:20 μsec/cm

Figure 4-5. 50-watt OCR integrator output during the -30 percent power transient.

4.2 50-WATT OCR - EFFICIENCY DISCUSSION

Of primary importance in the design of an optimum charge regulator is the efficiency of power transfer. In order to more effectively understand the losses in this circuit, the following discussion details each major area of dissipation and how improvements may possibly be made, while Table 4-2 summarizes the major dissipation areas.

4.2.1 Switching Circuit

The efficiency of this circuit is most important since it must transfer all of the power from the solar panel to the battery. For this reason, a detailed discussion of each of the major dissipation areas is given for this block.

Dissipation Area	Power Loss, watts	Discussion, paragraph
Switching Circuit		4.2.1
Bias Power	1.20	4.2.1.1
Q1 - Saturation	0.68	4.2.1.2
Q1 - Switching	2.63	4.2.1.3
Input Filter Inductor - L_1	0.80	4.2.1.4
Flyback Diode - CR1	0.68	4.2.1.5
Sensing Resistor	0.68	4.2.1.6
Switching Choke - Copper	1.36	4.2.1.7
Switching Choke - Core	1.54	4.2.1.8
Duty Factor Modulator	0.14	4.2.2
CSA, PHC, Bist. and Int.	0.16	4.2.2
Switching Regulator and Bias Converter	1.63	4.2.2
Hunting Loss	0.50	4.2.3
Total	12.00	
Power In = 50.0 watts Efficiency = 76 percent		

Table 4-2. Summary of power losses in the 50-watt OCR.

4.2.1.1 Bias Power. This power loss was determined by measuring the input power delivered by each of the four bias supplies. The total power included here is 1.20 watts. Most of the power (1.07 watts) is used for the drive for Q1, therefore, it would not be possible to reduce it by any significant amount.

4.2.1.2 Q1 - Saturation. This power loss can be determined from the general equation

$$P = \frac{RI_p^2 D}{3} \tag{4-2}$$

where

R = the saturation resistance of Q1

I_p = the peak collector current

D = the duty factor.

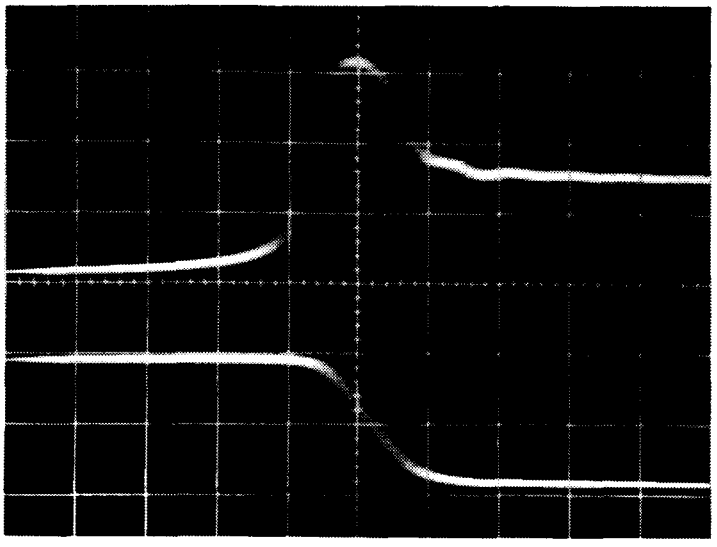
Using the values R = 0.03Ω, I_p = 18 amperes, and D = 0.21, the power dissipated due to the saturation resistance of Q1 is found to be 0.68 watts. It would be possible to reduce this loss by a factor of two by paralleling two power transistors. The total savings would be 0.34 watts.

4.2.1.3 Q1 - Switching. This loss can be approximated using the switching waveforms shown in the photograph of Figure 4-6. This photograph shows the collector emitter voltage and the collector current of Q1 at the moment that Q1 turns off. If the power is approximated by breaking the waveforms into segments, the result is as follows. For the first 0.75 μsec the voltage increases from 0 to 10 volts linearly while the current remains at 18 amperes. Therefore,

$$P\ (0 \rightarrow 0.75\ \mu\text{sec}) = \frac{5 \times 18 \times 0.75}{100} = 0.68 \text{ watts}$$

(a)

(b)



(a) V_{ce} (Q1) - Vertical:20 V/cm
(b) I_1 - Vertical:10 A/cm
} horizontal:0.2 μsec/cm

Figure 4-6. 50-watt OCR switching waveforms during the turn off of Q1.

From 0.75 to 0.85 μsec the voltage increases from 10 to 40 volts with the current at 18 amperes. Therefore,

$$P\ (0.75 \longrightarrow 0.85\ \mu sec) = \frac{25 \times 18 \times 0.1}{100} = 0.45\ watts$$

Finally for the next 0.3 μsec, the voltage averages about 50 volts while the current drops to zero. Therefore,

$$P\ (0.85 \longrightarrow 1.15\ \mu sec) = \frac{50 \times 100 \times 0.3}{100} = 1.5\ watts$$

The total power lost due to switching is 2.63 watts. About 0.5 watts could be saved by increasing the turn-off drive to Q1, thereby reducing the power lost during the first 0.75 μsec of switching.

4.2.1.4 Input Filter Inductor - L1. The DC drop across this choke was determined to be 0.4 volts and with 2 amperes in the choke, the power dissipated is 0.8 watt. By decreasing the copper loss in the choke this loss could be reduced but with the penalty of increased choke size. Assuming a decrease in series resistance of one half the present value, about 0.4 watts could be saved.

4.2.1.5 Flyback Diode - CR1. This loss can be approximated by using the equation given in paragraph 4.2.1.2. Using the values R = 0.03 ohm, I_p = 12 amperes, and D = 0.47, the power loss is found to be 0.68 watts. About one-half of this can be saved by paralleling two diodes. This results in a savings of 0.34 watts.

4.2.1.6 Sensing Resistor - R_s. The power lost in this resistor is the same as in CR1 since it has about the same resistance. Reduction of this resistor is not too practical for this decreases the magnitude of signal available to the current sensing amplifier and may lead to stability problems.

4.2.1.7 Switching Choke - Copper. This loss is due to the series resistance of the switching choke. This resistance is about 0.03 ohms in the primary and 0.03 ohms in the secondary. Therefore, it will have the same loss as determined for the combination of the saturated Q1 condition and CR1 or about 1.36 watts. It can be reduced by reducing the series resistance but a size and weight tradeoff would have to be made. Assuming a decrease of one-half the resistance, about 0.68 watts could be saved.

4.2.1.8 Switching Choke - Core. This loss is difficult to compute or measure accurately. Therefore, it was assumed to be the difference between the measured losses and the total power loss as determined from $P_{in} - P_{out}$.

4.2.2 Balance of Circuits

The balance of the circuits was found to dissipate about 1.93 watts. Savings in these areas is not practical as this power is divided among a large number of small circuits.

4.2.3 Hunting Loss

The power lost due to hunting was found to be 0.5 watt which met the goal of 2 percent which was initially set.

4.2.4 Summary

Based on the above described measurements, the total power dissipation was determined to be 12 watts with 50 watts input. The efficiency is found from these figures to be 76 percent which is 4 percent lower than the original goal of 80 percent.

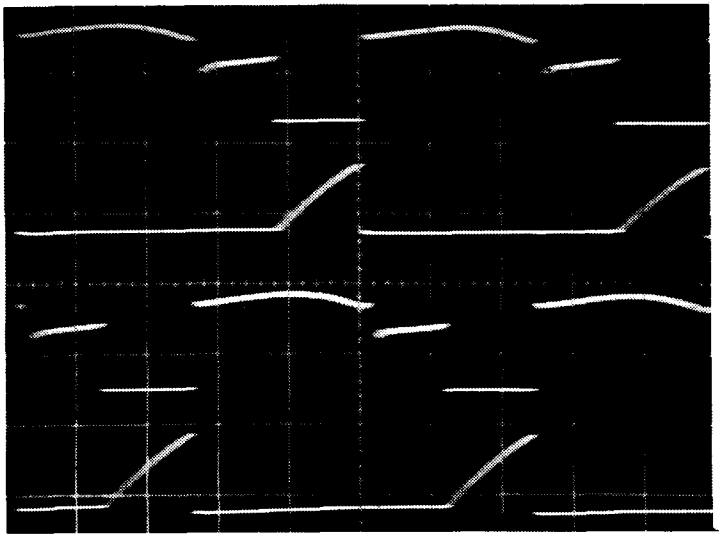
If the power savings as described were implemented, an additional 2.27 watts could be saved and this would raise the efficiency to 80.5 percent. It must be remembered, however, that this improvement would be at the cost of size and weight.

4.3 250-WATT REGULATOR EVALUATION

The operation of this unit also proved satisfactory in all respects and stability of operation was exhibited for all operating conditions.

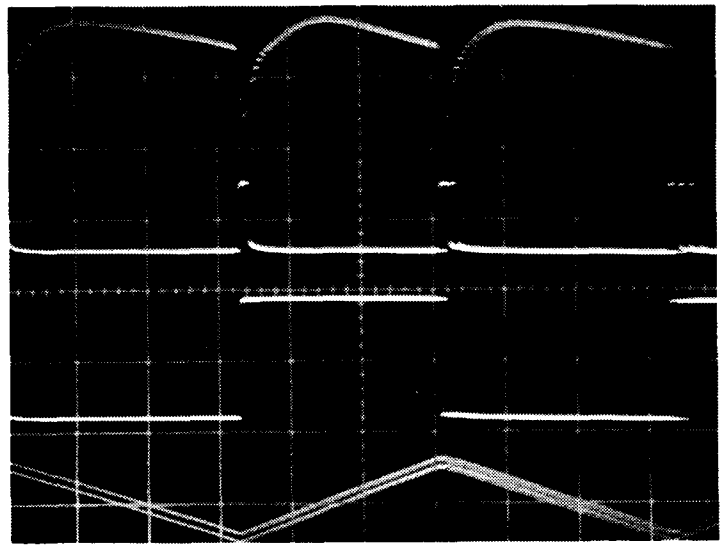
Figures 4-7 through 4-10 are photographs of some of the critical circuit waveforms. As described in the 50-watt regulator evaluation section, these photographs may be employed to determine some of the critical operating parameters and they are useful in calculating the hunting frequency.

Table 4-3 lists these parameters and the hunting frequency can be calculated with the design values as 64 hz, and 43 hz with the measured values. The actual hunting frequency can be determined from Figure 4-8 to be 32 hz. The difference between the hunting frequency calculated using the design values and the actual measured hunting frequency can be largely attributed to the integrator constant. The measured value is 1.6/second while the design value is 2.6/second.



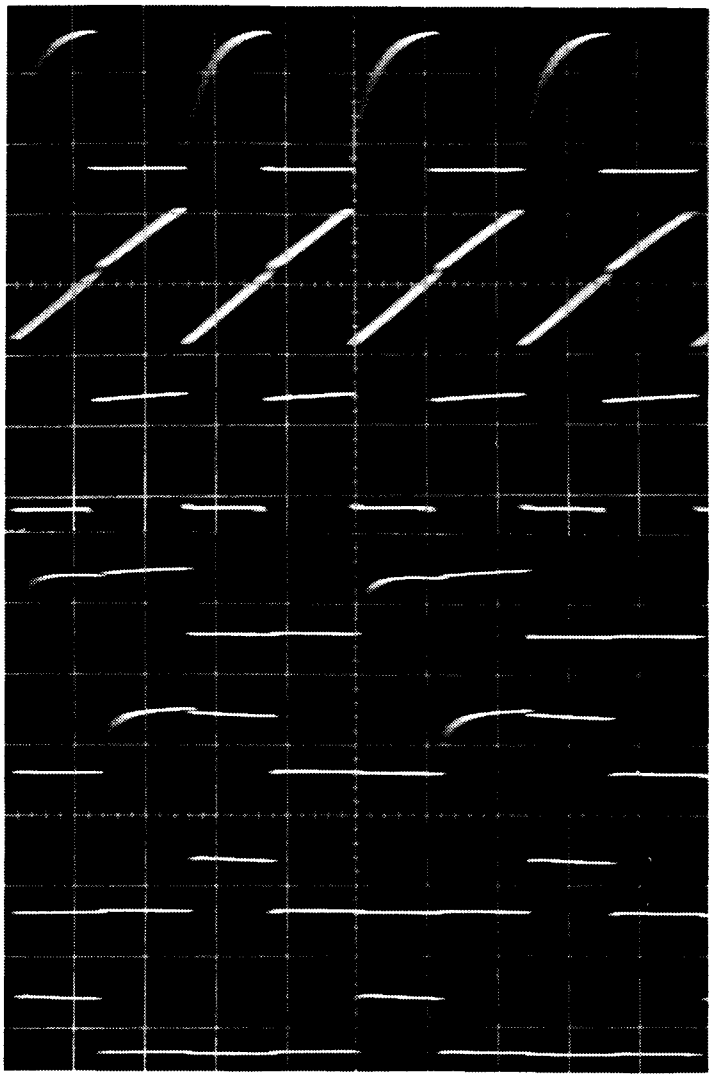
(a) V_{ce} (ϕA) - Vertical:50V/cm
(b) I_c (ϕA) - Vertical:20A/cm
(c) V_{ce} (ϕB) - Vertical:50V/cm
(d) I_c (ϕB) - Vertical:20A/cm
} horizontal:100 μsec/cm

Figure 4-7. 250-watt OCR switching circuit waveforms.



(a) Current Sensing Amplifier Output - Vertical:5V/cm
(b) Peak Holding Comparator Output - Vertical:10V/cm
(c) Bistable Output - Vertical:5V/cm
(d) Integrator Output - Vertical:0.5V/cm
} horizontal: 5msec/cm

Figure 4-8. 250-watt OCR control loop waveforms.



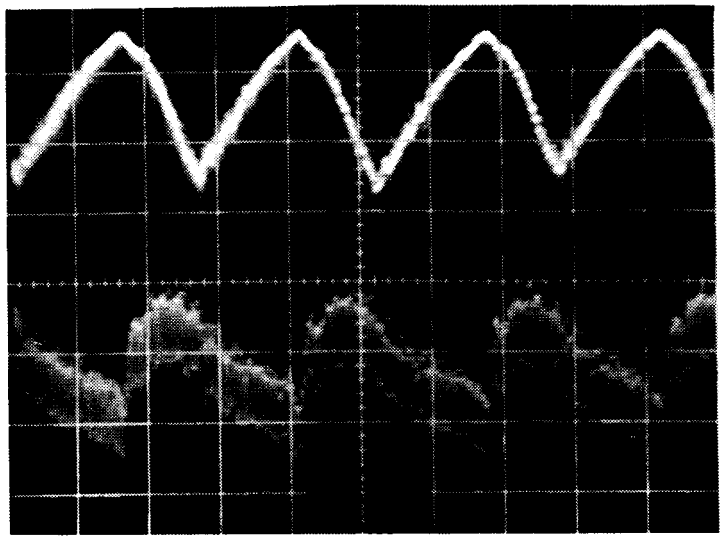
(a) Clock Output - Vertical:10V/cm
(b) Ramp Generator Output - Vertical:5V/cm
(c) Comparator Output - Vertical:10V/cm
(d) FF3-A - Vertical:10V/cm
(e) FF4-A - Vertical:10V/cm
(f) FF1-A - Vertical:10V/cm
(g) FF2-A - Vertical:10V/cm

} horizontal: 100 μsec/cm

Figure 4-9. 250-watt OCR duty factor modulator waveforms.

(a)

(b)



(a) ΔV_{sp} - Vertical:2V/cm
(b) ΔI_{sp} - Vertical:100MA/cm
} horizontal:10 msec/cm

Figure 4-10. 250-watt OCR solar panel output voltage and current.

4.4 250-WATT OCR EFFICIENCY DISCUSSION

The primary circuit losses are detailed in Table 4-4. The efficiency goal of 90 percent for this unit was not achieved. The measured efficiency was 82.5 percent, and this is somewhat short of the desired goal.

The losses, as listed in Table 4-4, were calculated in the same manner as for the 50-watt regulator. Upon examination of these figures, it can be seen that the single major loss appears to be in the switching chokes. If all of the other losses are examined, another 4 or 5 watts could be saved in these areas. In order to improve the efficiency, it is necessary to improve the core losses in the switching chokes. Various types of cores were considered for the design and a ferrite core was finally chosen as the one having the lowest losses per pound. Based on calculations it seems that the core loss should be less than 20 watts in the two chokes; however, the apparent loss is 20 watts. The mechanism for this loss is unknown at this time, but investigation will continue during the advanced study program.

Parameter	Design Value	How Determined	Measured Value	How Determined
Efficiency	0.9	Design Goal	0.82	$P_{out}/P_{in} + P_{hunting}$
Solar Panel Voltage - V_{sp}	45 volts	Nominal Design Value	43 volts	DC Measurement
Battery Voltage - V_B	40 volts	Nominal Design Value	40 volts	DC Measurement
Solar Panel Voltage Change - ΔV_{sp}	2.4 volts	$\Delta V_{sp} = \frac{\sqrt{2L_p f_s P}}{D_1^2 \sqrt{N}} \Delta D$	2 volts	Figure 4-9a
Primary Duty Factor	0.208	$D_1 = \frac{\sqrt{2L_p f_s P}}{D_1 \sqrt{N}}$	0.22	Figure 4-7a
Battery Current Change - ΔI_B	0.25 amp	Nominal Design Value	0.2 amp	AC Measurement
Integrator Constant - K	2.6/sec	Nominal Design Value	1.6/sec	Figure 4-8d and Figure 4-9b
Choke Primary Inductance	175 uh	Nominal Design	175 uh	- - - - - - - -

Table 4-3. Summary of circuit parameters for hunting frequency determination - 250-watt OCR.

Dissipation Area	Power Loss, watts
Switching Circuit	
Bias Power	3.1
Switching Transistors	
Saturation	1.0
Switching	2.8
Input Filter Inductor	2.1
Output Filter Inductor	1.7
Flyback Diodes	1.1
Sensing Resistor	2.1
Switching Chokes	
Copper	4.2
Core	20.0
Duty Factor Modulator	0.1
CSA, PHC, Bist, and Int.	0.1
Switching Regulator and Bias Converter	1.7
Hunting Loss	4.0
Total	44.0
Power In = 250 watts	
Efficiency = η = 82.5 percent	

Table 4-4. Summary of power losses in the 250-watt OCR.

5. BATTERY STUDY

The battery testing phase of the program was conducted in order to determine the effects of high frequency charging on battery performance. Nickel-cadmium, silver-cadmium, and silver-zinc batteries were charged at several different frequencies between 100 Hz and 100K Hz. Direct current was superimposed on the alternate current and was of such value that it equaled the required current for a prescribed orbit. The batteries were then discharged with dc which was also of such magnitude that it corresponded to the same prescribed orbit. A d-c charge was used at the beginning and end of the cycling procedure for comparison. The effects of charging efficiency was observed in this manner, and in the case of the silver-zinc battery, the effect of high frequency on the time a cell charged on the lower silver plateau was noted.

The waveform used in the battery testing was a simple sinewave. This did not conform to the waveform used in the O.C.R., but it is doubtful that this difference in waveform would have any effect on battery characteristics. In addition, vented cells were used on this program, whereas sealed cells would have to be used for actual missions, since nothing was likely to be gained by using the more expensive sealed cells.

The batteries to be charged by the non-dissipative charge regulator were designed for one of the two orbits of Case I and one of the two orbits of Case II. The Case I orbit is a highly elliptical orbit (apogee and perigee 45,000 miles and 200 miles, respectively) and the Case II orbit is a circular, 300-mile orbit. Orbital conditions were designed for each system and batteries were then selected to perform within the power available from the solar panel-power transfer system. All pertinent characteristics of the batteries were considered in the designs, and some consideration was given to the third electrode designs in Case II as a possible means of lowering battery weight.

5.1 BATTERY DESIGN

Case I

This involves the use of a spin stabilized satellite in a highly elliptical earth orbit. Approximately 50 watts of power are available at the solar panel output terminals. Output voltage will range from 20 to 30 volts.

The orbital periods for Case I are summarized below:

Orbit	A	B
Apogee	45,000 miles	200,000 miles
Perigee	200 miles	1,000 miles
Orbital period	21.0 hours	234 hours
Dark time/orbit	1.0 hour	16 hours
Charge time/orbit	20.0 hours	218 hours
Orbits/year	418	37.5

Since the dark time to light time ratio is relatively small, the optimum constant power load level for this case can approach the maximum power level available for recharging. With a maximum solar panel output of 50 watts and a charge regulator efficiency of 80 to 90 percent, the power available for recharging the battery will be 40 to 45 watts.

Batteries selected for this application and the conditions under which they must operate are summarized in Tables 5-1 and 5-2. For Orbit A, cells have been selected on the basis of the discharge current, depth of discharge and operating temperature range. In order to prevent the minimum voltage from falling below 12.0 volts, the plateau voltage of a silver-cadmium cell under discharge cannot fall below 0.92 volt. This potential can be maintained at -20°C even at the C rate, as shown in Figure 5-1. Similarly, in order to prevent the minimum voltage from falling below 12.0 volts, the plateau voltage of a silver-zinc cell, under discharge should not fall below 1.33 volts. Figure 5-2, therefore, shows that at -20°C this type of cell should not be discharged at rates greater than 0.5C. Although

Cell Type	Cell Capacity Amp-Hrs	Discharge Amp-Hrs	Percent Depth of Discharge	Number of Cells	Battery Weight (lbs)	OCR Output (watts)	Charging				Discharging			
							Time (hrs)	Average Watts	Volts	Average Amps	Time (hrs)	Watts	Volts	Amps
AgCd	10	2.7	27.0	13	6.9	40	20	2.25	20.8	0.11	1.0	37.75	13.9	2.7
AgCd	10	3.05	30.5	13	6.9	45	20	2.5	20.8	0.12	1.0	42.5	13.9	3.15
AgZn	7.5	2.8	37.4	9	3.0	40	20	2.25	18.5	0.12	1.0	37.75	13.5	2.8
AgZn	7.5	3.15	42.0	9	3.0	45	20	2.5	18.5	0.135	1.0	42.5	13.5	3.15

Table 5-1. Case I, Orbit A, (100 cycles per year).

Cell Type	Cell Capacity Amp-Hrs	Discharge Amp-Hrs	Percent Depth of Discharge	Number of Cells	Battery Weight (lbs)	OCR Output (watts)	Charging				Discharging			
							Time (hrs)	Average Watts	Volts	Average Amps	Time (hrs)	Watts	Volts	Amps
AgCd	100	43.2	43	12	41	40	218	4	19.2	0.20	16	36	13.2	2.7
AgCd	100	49.6	50	12	41	45	218	4	19.2	0.20	16	41	13.2	3.1
AgZn	100	41.6	42	9	25	40	218	4	18.5	0.21	16	36	13.5	2.6
AgZn	100	48.0	48	9	25	45	218	4	18.5	0.21	16	41	13.5	3.0

Table 5-2. Case I, Orbit B, (38 cycles per year).

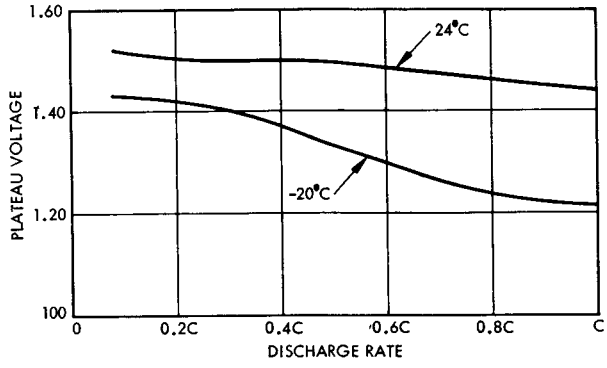


Figure 5-1. Silver-cadmium cell discharge rate as a function of plateau voltage.

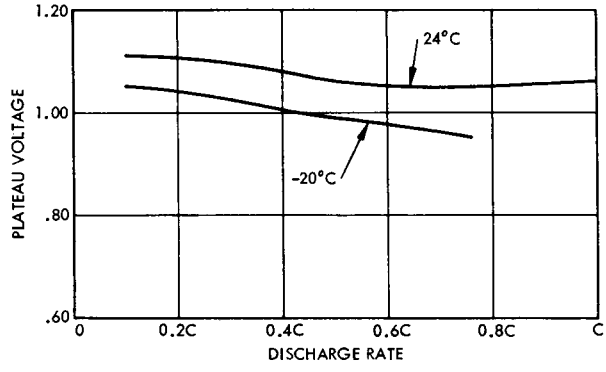


Figure 5-2. Silver-zinc cell discharge rate as a function of plateau voltage.

smaller cell sizes are possible with proper thermal conditioning of the battery, the cell size selection is also controlled by the permissible depth of discharge. For satisfactory battery performance over a minimum of 100 charge-discharge cycles, the depth of discharge should not exceed 50 percent.

In the case of Orbit B, cell selection has been determined by the power requirements during discharge with the depth of discharge limited to 50 percent or less. The percent of battery capacity as a function of temperature and rate of discharge is shown in Figure 5-3 for a silver-cadmium cell and in Figure 5-4 for a low-rate, silver-zinc cell.

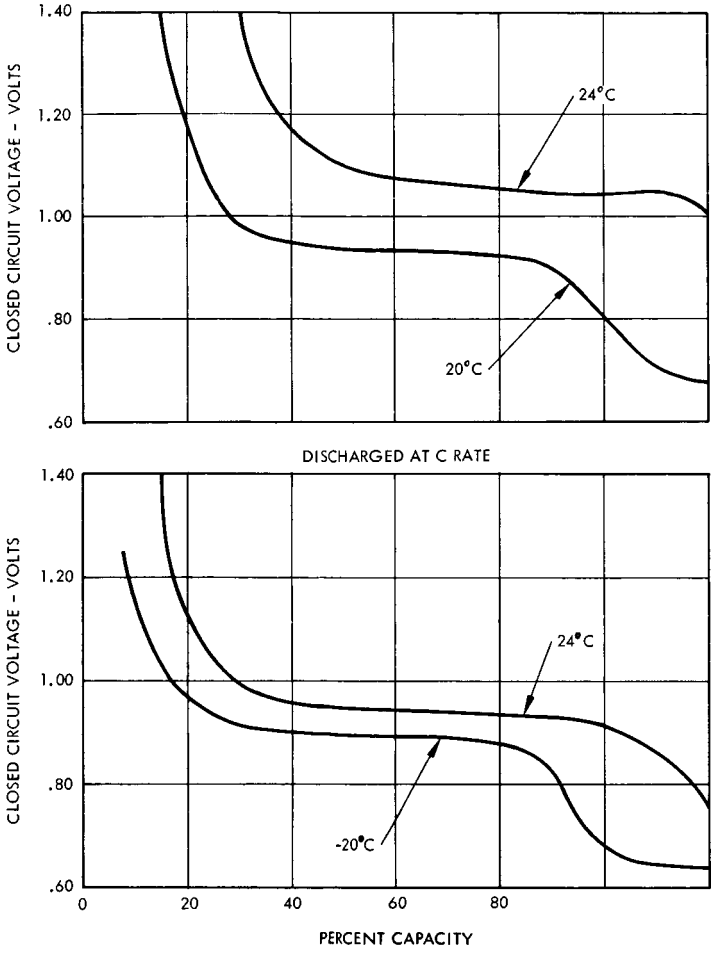


Figure 5-3. Silver-cadmium cell battery capacity as a function of rate of discharge.

For both orbits, the number of cells for each battery system has been defined by the minimum discharge voltage level established for battery operation. In the case of silver-cadmium, a nominal voltage of 1.07 volts per cell was used, and in the case of silver-zinc this nominal voltage was 1.5 volts per cell. For the silver-cadmium system, a battery pack of 13 series-connected cells is needed. With the silver-zinc system, the number of cells can be reduced to nine, resulting in an appreciable reduction in battery weight.

It should be noted that although the battery systems for Orbit B weigh six times as much as for Orbit A, approximately 30 times as much power is available during the dark period of Orbit B than during Orbit A. Usable capacities are 0.2 to 0.3 AHR/lb for Orbit A and 1 to 2 AHR/lb for Orbit B.

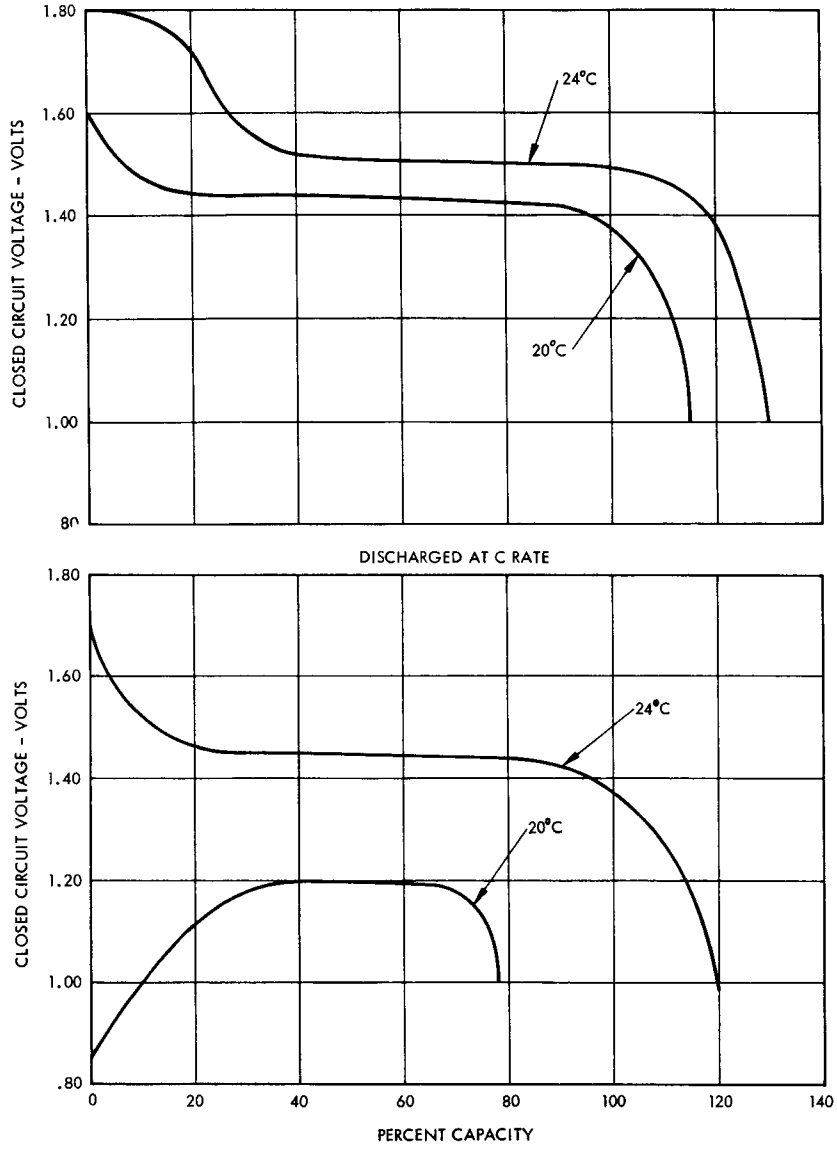


Figure 5-4. Silver-zinc cell battery capacity as a function of rate of discharge.

5.2 CASE II

This involves the use of an oriented solar cell array in a circular earth orbit. Approximately 250 watts of power are available at the solar panel output terminals. Output voltage will range from 40 to 50 volts.

Orbital periods for the circular earth orbit of Case 2 were derived from Figure 5-5 and are summarized as follows:

Orbital distance	300 miles	600 miles
Orbital period	1.55 hours	1.70 hours
Dark time/orbit	0.59 hours	0.57 hours
Charge time/orbit	0.96 hours	1.13 hours
Orbits/day	15.5	14.1
Orbits/year	5651	5153

Sealed, sintered-plate, nickel-cadmium cells were selected for this application. The optimum constant power load levels were determined for each orbital distance. These values assume a 25-percent overcharge in order to return the cell to maximum capacity. With a maximum solar panel output of 250 watts and a charge regulator efficiency of 80 to 90 percent, the power available for recharging will be between 200 and 225 watts.

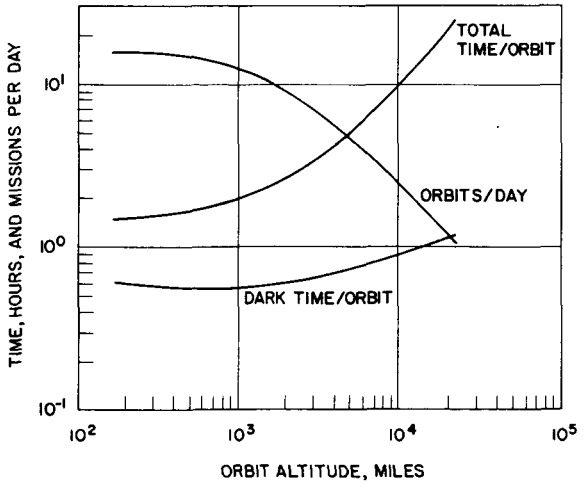


Figure 5-5. Orbital data.

The optimum constant power load levels were determined by consideration of the following factors:

1. The satellite power load levels are identical during the light and dark periods of each orbit.
2. For complete recharge, 125 percent of battery capacity removed must be returned.

The following simplified relationship was derived to enable optimum power levels to be calculated:

$$t_c (P_T - P_d) \eta_i = t_d P_d \qquad (5\text{-}1)$$

where

P_T = Total power available from optimum charge regulator

P_d = Watts available during charge or discharge

t_c = Time for charging, hours

t_d = Time for discharge, hours

η_i = Current efficiency, assumed to be 0.80

For the 300-mile orbit, a 200-watt recharge capability would allow a maximum continuous discharge of 113 watts during the entire orbit and assure complete recharge of the battery during the light or recharge period of the orbit. By increasing this recharge capability to 225 watts, the maximum continuous discharge level would be increased to 127 watts. For the 600-mile orbit, 123 watts could be discharged and recharged at 200 watts or 138 watts could be discharged if recharged at the 225-watt level.

The number of cells required for the mission was based on a discharge voltage of 1.2 volts per cell at 25°C and a battery operating voltage range of 25 to 34 volts. A series connected 28-cell nickel-cadmium battery would show 33.6 volts during discharge at 25°C. Under load at -20°C, this battery voltage would be reduced by approximately 0.1 volt per cell to 30.8 volts. Similarly a 22 cell battery would produce 26.4 volts at 25°C and 24.2 volts at -20°C under load.

The size of each battery cell was determined by the optimum charge rate with the depth of discharge limited to 50 percent. Batteries selected for this application and the conditions under which they must operate are summarized in Tables 5-3 and 5-4. A charging rate of C/15 has been assumed.

Size "A" corresponds to the conventional cell and its size was determined by multiplying the optimum charge current by 15. This is the minimum cell size for charging at the C/15 rate. Sealed nickel-cadmium cells are also available with a "third electrode" (General Electric) or "adhydrode" (Gulton). This type of cell allows higher charge rates (C/2) without increasing internal cell pressure. Evolved gases are caused to recombine at a rate in equilibrium with the rate of evolution. Size "B" corresponds to this type of cell. Its size was determined by multiplying the charge current by 2. Another method that permits higher charge rates is the "Stabister" system (Sonotone-Mallory). This is a dual diode circuit which diverts excess charge current around fully charged cells. Since a smaller, lighter battery could be used with a minimum loss of time for recharging, these cells should be considered.

Recent conversations with Sonotone have centered around the use of coulometers for measuring battery state-of-charge as well as for limiting overcharge.

5.3 TEMPERATURE EFFECTS

Battery characteristics during charge and discharge are affected by the ambient temperature. A review of recent NAD Crane and Inland Test Laboratories reports (QE/C 65-356 and NAS 5-1048, 1965) leads to the conclusion that both cell capacities and cycle life are detrimentally affected by high temperatures. Figure 5-6, Battery capacity versus temperature, illustrates the fact that temperatures above 25°C immediately reduce the initial capacity of nickel-cadmium cells. A further observation is that less than 50 percent of rated capacity remains after 4200 cycles at 1.5 hours each when a temperature of 40°C is used. It is recommended, therefore, that ambient temperatures of nickel-cadmium batteries be confined to the range of -20° to +40°C.

Number of Cells	OCR Output (watts)	Charging				Discharging			
		Time (hrs)	Watts	Volts	Amps	Time (hrs)	Watts	Volts	Amps
22	200	0.96	87	31.5	2.76	0.59	113	26.4	4.25
22	225	0.96	98	31.5	3.11	0.59	127	26.4	4.80
28	200	0.96	87	40.0	2.17	0.59	113	33.6	3.36
28	225	0.96	98	40.0	2.45	0.59	127	33.6	3.80

Number of Cells	OCR Output (watts)	Cell Size "A"				Cell Size "B"			
		Capacity Amp-Hrs	Percent Depth of Discharge	Discharge Amp-Hrs	Battery Weight (lbs)	Capacity Amp-Hrs	Percent Depth of Discharge	Discharge Amp-Hrs	Battery Weight (lbs)
22	200	41	5	2.50	105	6.5	39	2.50	14.3
22	225	46	5	2.83	121	7.4	39	2.83	16.3
28	200	32	5	1.98	109	5.2	38	1.98	14.5
28	225	37	5	2.25	123	5.8	39	2.25	15.2

Table 5-3. Case II, 300 mile orbit.

Number of Cells	OCR Output (watts)	Charging				Discharging			
		Time (hrs)	Watts	Volts	Amps	Time (hrs)	Watts	Volts	Amps
22	200	1.13	77	31.5	2.44	0.57	123	26.4	4.64
22	225	1.13	87	31.5	2.76	0.57	138	26.4	5.20
28	200	1.13	77	40.0	1.92	0.57	123	33.6	3.67
28	225	1.13	87	40.0	2.17	0.57	138	33.6	4.11

Number of Cells	OCR Output (watts)	Cell Size "A"				Cell Size "B"			
		Capacity Amp-Hrs	Percent Depth of Discharge	Discharge Amp-Hrs	Battery Weight (lbs)	Capacity Amp-Hrs	Percent Depth of Discharge	Discharge Amp-Hrs	Battery Weight (lbs)
22	200	36	6	2.65	97	5.8	46	2.65	12.8
22	225	41	6	2.95	105	6.5	46	2.95	14.3
28	200	28	6	2.10	95	4.6	46	2.10	12.8
28	225	32	6	2.34	109	5.2	45	2.34	14.5

Table 5-4. Case II, 600 mile orbit.

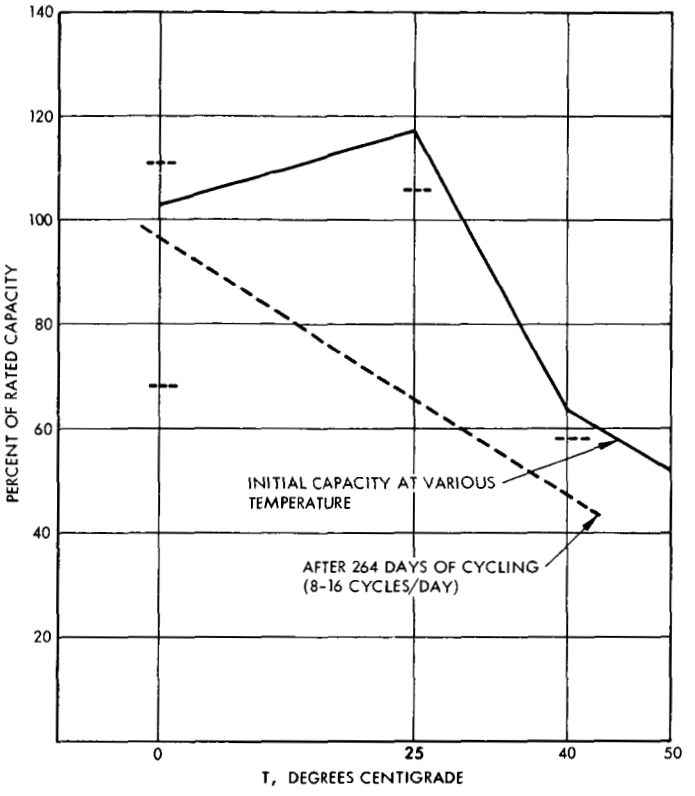


Figure 5-6. Battery capacity versus temperature.

The silver-zinc and silver-cadmium batteries being considered in Case I encounter similar temperature effects. The rate of self-discharge must be considered during the long charge period (i.e., 20 and 218 hours). Storage of batteries at temperatures of 70°C (160°F) results in a capacity loss of 50 percent in two days. A reasonable temperature range for future experiments is -20° to +25°C. At 40°C, the capacity loss would be 1.0 to 1.5 percent per day.

5.4 BATTERY TESTING PROGRAM

The battery testing phase of the project was designed to determine the effects of the optimum charge regulator on battery performance. The particular concern was the possible effect of a high frequency component on charging efficiency.

Silver-cadmium and silver-zinc cells were used for testing in a simulated Case I, Orbit A, and nickel-cadmium cells were used for the

simulated Case II, 300-mile orbit. A sufficient number of cells were bought to complete batteries and have enough remaining for testing. There were purchased 120, 23-ampere per hour nickel-cadmium; 35, 7.5-ampere per hour silver-zinc; and 45, 10-ampere per hour silver-cadmium cells. In the case of the nickel-cadmium cells, each battery consists of two series-connected modules wired in parallel because of the requirement for a 46-ampere per hour battery. This cell construction was implemented since 23 ampere per hour cells were readily available.

The test procedure is outlined in Table 5-5.

Cell Type	Cells per Battery	t_c, hours	I_c, amps	I_d, amps
Ni-Cd	8	1	2.17 ±0.7	2.40
Ag-Cd	8	20	0.110 ±0.040	2.7
Ag-Zn	6	20	0.140 +0.040	2.8

Table 5-5. Test procedure.

In Table 5-5, t_c is the charge time in hours, I_c is the charge current (DC ± AC) in amperes, and I_d is the discharge current (DC) in amperes. Following the value of the charge current is the figure designating the amplitude of the AC sine wave. Thus, for the nickel-cadmium charging tests the mean value was 2.17 amperes but the current varied from 2.17 ±0.7 amperes. Before the AC charging commenced with each battery, it was charged with DC at the mid-point value for a reference point. Following the initial DC charging, subsequent charge cycles were done at 0.1 khz, 1 khz, 10 khz, and 100 khz, except for the nickel-cadmium cells. Due to the higher currents drawn with these cells, 30 khz was the highest frequency the charger could provide. After these tests were completed, a final DC charge was made to determine if there were any permanent effects of the AC charging. In some cases additional DC charges were also made.

5.4.1 Instrumentation

The battery tester consists of a charge-discharge circuit, voltage sensor, and timing logic. The tester operates as follows:

5.4.1.1 Charge/Discharge Circuit. The charge/discharge circuit, as shown in Figure 5-7, consists of a sense amplifier, two voltage references, and two power amplifiers. The voltage references are zener diodes; the reference for the charge circuit includes provision for modulation of the charge current by means of an external oscillator. The power amplifiers are high current gain units composed of silicon power transistors. The power amplifier for the charger uses high frequency transistors to obtain wide bandwidth so that the higher modulation frequencies can be accommodated. The circuit for both modes is closed loop feedback amplifiers utilizing a 1-ohm sensing resistor to maintain constant output in spite of battery voltage and impedance.

5.4.1.2 Voltage Sensor. The voltage sensor consists of a high gain direct coupled amplifier and a voltage reference. The battery voltage is compared to the voltage reference. When the battery voltage drops below a preset level, a relay is made to actuate, signalling the presence of low voltage and automatically terminating the discharge. The time allowed for the discharge part of the cycle is, in all cases, long enough that the cut-off level will be reached. During the charge part of the cycle, voltages in excess of this cut-off level will always be maintained.

5.4.1.3 Timing Logic. Charge or discharge mode is selected by relays; the preset value of each current is automatically selected alternately, one hour for each, on a recycle basis. Should the voltage sensor signal an insufficient battery voltage during a discharge cycle, the discharge is terminated and the balance of the hour is spent on open circuit. Running time meters record actual charge and discharge time.

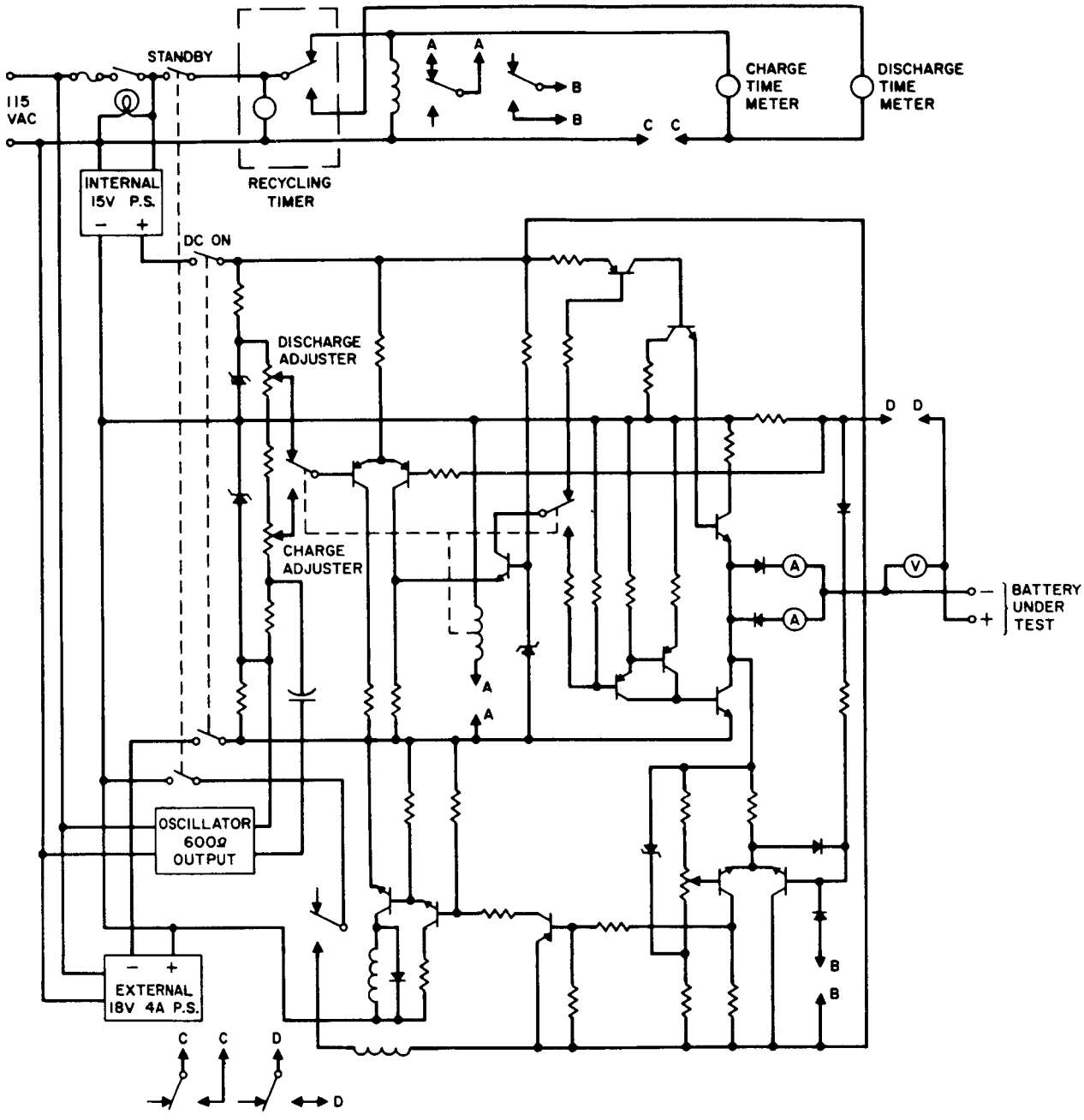


Figure 5-7. Schematic diagram.

5.4.2 Results of Silver-Cadmium Battery Test

The current efficiencies, η_i, for the silver-cadmium battery were lower than anticipated, although they did increase somewhat, as can be seen in Table 5-6 with cycling. Beginning with the fifth cycle, it is noticed that the d-c charges resulted in current efficiencies of 0.96 ± 0.01 and that the charges with an a-c component were decidedly lower. There is no efficiency trend with frequency, however, and considering all of the results it is difficult to draw the conclusion that the a-c component adversely affected the charge efficiency. Such an effect would be difficult to understand since it was definitely not found for the silver-zinc or nickel-cadmium batteries, and the silver-cadmium has an electrode common to each of the two other batteries.

F, hz	t_c, hrs	t_d, hrs	$t_d I_d$, amp hrs	η_i
D.C.	20.0	0.56	1.50	0.68
100	20.0	0.67	1.80	0.82
D.C.	20.0	0.73	1.97	0.89
1000	20.0	0.76	2.06	0.94
D.C.	20.1	0.78	2.12	0.96
100	20.0	0.71	1.91	0.87
D.C.	20.0	0.79	2.14	0.97
1000	20.0	0.74	1.99	0.91
10^4	20.0	0.71	1.92	0.87
10^5	20.1	0.73	1.98	0.89
D.C.	20.0	0.77	2.08	0.95

Charge Current, I_c = 0.110 ± 0.040 amps
Discharge Current, I_d = 2.70 amps
Discharge Cut-Off = 8.0 volts

Table 5-6. Silver-cadmium battery, 8-cells.

An interesting observation made about the silver-cadmium battery cycling was that the upper silver plateau was never reached. Discharge was terminated at 8 volts (1 volt per cell) and only 22 percent of the nominal capacity was charged back from that point. Since all of the charging was done along the lower silver plateau, the battery operated with very high voltage efficiency. Charging occurred at 9.2 to 9.5 volts (1.15 to 1.19 volts per cell) and most of the discharge occurred at about 8.6 volts, for a mean voltage efficiency of more than 90 percent. Since the upper silver plateau was never reached, the battery voltage for the 13-cell battery of Case I, Orbit A would be no more than 15.4 volts, instead of 20.8 volts as indicated in Table 5-1.

5.4.3 Results of Silver-Zinc Battery Test

Table 5-7 shows the results of the silver-zinc battery testing. It is noted that current efficiencies were very high and were dropping slightly with cycling but there was no indication that the a-c component was affecting this efficiency. There was visible deterioration of the cells by the sixth cycle, but this is normal for this type of cell. Most secondary silver-zinc batteries have only a limited amount of recharge ability.

An interesting observation was made concerning the time to reach the upper silver plateau during the charging operations. In the following table the times required to reach the upper silver plateau are shown. In Table 5-8, the column headed f, hz, is the frequency in hertz. The columns headed E_1, E_2, etc., refer to the time in hours required for the first, second, etc., electrodes to reach the upper charging plateau. Since the charge was always terminated at 20 hours, not all electrodes reached the second charging plateau. In fact, on the first charge, only one electrode did and it reached that point only a few minutes before the charging was stopped. It was seen that at higher frequencies, more electrodes reached the upper plateau and reached it earlier. On the final d-c charge, this trend was reversed and only three electrodes reached the second plateau, but the situation was worse than it was with the original d-c charge. It would appear that high frequency charging

f, hz	t_c, hours	t_d, hours	$t_d I_d$, amp-hours	η_i
d-c	20.0	1.01	2.83	1.01
100	20.4	1.02	2.86	1.00
1000	20.0	0.99	2.78	0.99
10^4	20.0	0.99	2.78	0.99
10^5	20.0	0.98	2.76	0.98
d-c	20.0	0.98	2.76	0.98
Charge Current, I_c = 0.140 ± 0.040 amps				
Discharge Current, I_d = 2.80 amps				
Discharge Cut-Off = 8.5 volts				

Table 5-7. Silver-zinc battery, 6-cells.

f, hz	E_1	E_2	E_3	E_4	E_5	E_6
d-c	19.9					
100	xx	xx	xx	xx	xx	xx
1000	18.9	19.6				
10^4	18.7	19.2				
10^5	18.2	18.3	18.6	19.7		
d-c	18.5	18.6	18.8			

Table 5-8. Time of charge on lower silver plateau.

has a small but definite adverse effect on charge acceptance on the lower silver plateau. This effect did not show up with the silver-cadmium testing since only 22 percent of nominal capacity was charged into those cells, whereas 37 percent of the nominal capacity was charged into the silver-zinc cells.

One interpretation of Table 5-7 is that a given column represents the effects of a given electrode in every case. This may be true but since individual electrodes were not monitored it was not possible to show this. The fact that an electrode moved from one silver

plateau to the next was shown by a sharp voltage jump in the battery of about 0.25 volt.

5.4.4 Results of Nickel-Cadmium Battery Test

The results of the nickel-cadmium battery testing are given in Tables 5-9 through 5-14. It will be seen that η_i is seldom less than 100 percent and is often higher than 100 percent. Current efficiencies in excess of 100 percent are commonly found with nickel-cadmium batteries. Some of the active materials only slowly react and for one cycle (and for many cycles when the depth-of-discharge is very low, as it is in this case) a considerable amount of that material can be realized. But for many deep discharges, of course, the maximum value of η_i is 100 percent.

It is clear when examining the tables for the nickel-cadmium tests that the efficiencies were very high and unaffected by either cycling or high frequency charging. High current efficiency is generally not a strong point of nickel-cadmium cells, but when the depth-of-discharge is very low (about 6-1/2 percent in this case) than the current efficiency is normally very high.

The discharge current was changed from 3.36 to 2.40 amperes in order to coincide exactly with the battery designed for the 300-mile orbit of Case II, with 225 watts from the OCR. The discharge current is given in Table 5-3 as 4.80 amperes, but the battery capacity is given as 46 ampere-hours. Since our cells are only 23 ampere-hours, this discharge current had to be 2.40 amperes. Some results of a limited amount of cycling at 3.36 amperes discharge are also included.

5.5 GENERAL CONCLUSIONS

The results of the battery testing program would indicate that, under the conditions prevailing during the testing, the high frequency component has no degrading effects. A possible exception is the effect noted previously for the time of charging on the lower silver plateau with silver electrode cells. But it ought to be born in mind that the nickel-cadmium cells were cycled at a very shallow depth of discharge.

When cycled at greater depths of discharge these cells notoriously go into an overcharge condition and yield rather poor current efficiencies. Further work should be done to determine if the high frequency component has any effect under conditions of greater depth of discharge. More extensive work should also be done to clarify the effects noted on silver electrodes.

The prime emphasis in this study program was the optimum charge regulator design. The battery study was only carried far enough to determine the effects of an OCR on the battery performance. For this reason, a minimum effort was expended on the battery study phase.

t_c, Hrs	$t_c I_c$, Amp-Hrs	t_d, Hrs	$t_d I_d$, Amp-Hrs	η_i	Remarks
0.97	2.10	0.66	2.22	1.06	D-C charge
0.97	2.10	0.66	2.22	1.06	
0.97	2.10	0.65	2.18	1.04	
0.97	2.10	0.62	2.08	0.99	
0.97	2.10	0.64	2.15	1.02	
0.97	2.10	0.63	2.12	1.01	
0.97	2.10	0.59	1.98	0.94	
0.97	2.10	0.64	2.15	1.02	
0.97	2.10	0.64	2.15	1.02	

Charge Current, I_c	=	2.17 ± 0.70 amps
A-C Component Frequency	=	100 hz
Discharge Current, I_d	=	3.36 amps
Discharge Cut-off	=	8.0 volts

Table 5-9. Nickel-cadmium battery, 8 cells.

t_c, Hrs	$t_c I_c$, Amp-Hrs	t_d, Hrs	$t_d I_d$, Amp-Hrs	η_i	Remarks
0.96	2.08	0.63	2.12	1.02	
0.97	2.10	0.56	1.88	.90	
0.97	2.10	0.63	2.12	1.01	
0.97	2.10	0.63	2.12	1.01	
0.97	2.10	0.55	1.85	.88	
0.97	2.10	0.64	2.15	1.02	
0.97	2.10	0.63	2.12	1.01	
0.97	2.10	0.63	2.12	1.01	
0.97	2.10	0.63	2.12	1.01	
0.97	2.10	0.63	2.12	1.01	
0.97	2.10	0.63	2.12	1.01	
0.97	2.10	0.63	2.12	1.01	
0.97	2.10	0.64	2.15	1.02	
0.97	2.10	0.63	2.12	1.01	
0.97	2.10	0.63	2.12	1.01	

Charge Current, I_c	=	2.17 ± 0.70 amps
A-C Component Frequency	=	1K hz
Discharge Current, I_d	=	3.36 amps
Discharge Cut-off	=	8.0 volts

Table 5-10. Nickel-cadmium battery, 8 cells.

t_c, Hrs	$t_c I_c$, Amp-Hrs	t_d, Hrs	$t_d I_d$, Amp-Hrs	η_i	Remarks
0.97	1.51	0.92	2.21	1.46	D-C charge
0.96	1.49	0.59	1.42	0.95	
0.96	1.49	0.62	1.49	1.00	
0.96	1.49	0.60	1.44	0.97	
0.96	1.49	0.63	1.51	1.01	
0.96	1.49	0.63	1.51	1.01	
0.96	1.49	0.63	1.51	1.01	
0.96	1.49	0.63	1.51	1.01	
0.96	1.49	0.62	1.49	1.00	
0.96	1.49	0.50	1.20	0.80	
0.96	1.49	0.62	1.49	1.00	
0.96	1.49	0.63	1.51	1.01	
0.97	1.51	0.63	1.51	1.01	

Charge Current, I_c	=	1.555 ± 0.50 amps
A-C Component Frequency	=	100 hz
Discharge Current, I_d	=	2.40 amps
Discharge Cut-off	=	8.0 volts

Table 5-11. Nickel-cadmium battery, 8 cells.

t_c, Hrs	$t_c I_c$, Amp-Hrs	t_d, Hrs	$t_d I_d$, Amp-Hrs	η_i	Remarks
0.96	1.50	0.63	1.51	1.01	D-C charge
0.96	1.50	0.62	1.49	0.99	
0.97	1.51	0.66	1.58	1.05	
0.96	1.50	0.64	1.54	1.03	
0.97	1.51	0.64	1.54	1.02	
0.96	1.50	0.63	1.51	1.01	
0.97	1.51	0.63	1.51	1.00	
0.97	1.51	0.63	1.51	1.00	
0.96	1.50	0.63	1.51	1.01	
0.97	1.51	0.62	1.49	0.99	
0.97	1.51	0.63	1.51	1.00	
0.96	1.50	0.63	1.51	1.01	
0.97	1.51	0.63	1.51	1.00	

Charge Current, I_c	=	1.555 $\pm$ 0.50 amps
A-C Component Frequency	=	1K hz
Discharge Current, I_d	=	2.40 amps
Discharge Cut-off	=	8.0 volts

Table 5-12. Nickel-cadmium battery, 8 cells.

t_c, Hrs	t_cI_c, Amp-Hrs	t_d, Hrs	t_dI_d, Amp-Hrs	η_i	Remarks
0.96	1.50	0.63	1.51	1.01	D-C charge
0.97	1.51	0.63	1.51	1.00	
0.97	1.51	0.63	1.51	1.00	
0.97	1.51	0.63	1.51	1.00	
0.97	1.51	0.63	1.51	1.00	
0.97	1.51	0.63	1.51	1.00	
0.97	1.51	0.63	1.51	1.00	
0.97	1.51	0.63	1.51	1.00	
0.97	1.51	0.63	1.51	1.00	
0.97	1.51	0.63	1.51	1.00	
0.97	1.51	0.63	1.51	1.00	
0.97	1.51	0.63	1.51	1.00	
0.97	1.51	0.63	1.51	1.00	

Charge Current, I_c	=	1.555 $\pm$ 0.50 amps
A-C Component Frequency	=	10K hz
Discharge Current, I_d	=	2.40 amps
Discharge Cut-off	=	8.0 volts

Table 5-13. Nickel-cadmium battery, 8 cells.

t_c, Hrs	$t_c I_c$, Amp-Hrs	t_d, Hrs	$t_d I_d$, Amp-Hrs	η_i	Remarks
0.96	1.50	0.63	1.51	1.01	D-C charge
0.96	1.50	0.63	1.51	1.01	
0.97	1.51	0.62	1.49	0.99	
0.96	1.50	0.62	1.49	0.99	
0.96	1.50	0.62	1.49	0.99	
0.97	1.51	0.62	1.49	0.99	
0.96	1.50	0.63	1.51	1.01	
0.96	1.50	0.63	1.51	1.01	
0.97	1.51	0.63	1.51	1.00	
0.96	1.50	0.62	1.49	.99	
0.96	1.50	0.63	1.51	1.01	
0.96	1.50	0.62	1.49	.99	

Charge Current, I_c	=	1.555 ± 0.50 amps
A-C Component Frequency	=	30K hz
Discharge Current, I_d	=	2.40 amps
Discharge Cut-off	=	8.0 volts

Table 5-14. Nickel-cadmium battery, 8 cells.